Synopsys Announces Immediate Availability of Broad Portfolio of Interface IP for TSMC's 20SoC Process

Silicon-proven Synopsys IP Portfolio on TSMC's 20SoC Process Technology Enables Designers to Reduce Power Consumption and Increase Performance for Mobile and Multimedia SoC Designs

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Highlights:

- Synopsys's DesignWare® IP portfolio for TSMC 20SoC includes USB, DDR, PCI Express®, and MIPI® PHY IP
- Silicon-proven IP portfolio has been designed into multiple customers' SoCs which are ramping to production now
- TSMC's 20SoC process enables designers to reduce the power consumption by up to 25 percent or increase performance by 30 percent
- Both process and IP have been optimized for mobile applications such as tablets and smartphones

Synopsys, Inc. (Nasdaq:SNPS), a global leader providing software, IP and services used to accelerate innovation in chips and electronic systems, today announced the availability of a range of DesignWare Interface IP on TSMC's 20-nanometer (nm) system-on-chip (SoC) process. The silicon-proven Synopsys DesignWare USB, DDR, PCI Express and MIPI PHY IP on TSMC's 20SoC process reduces risk for designers who need to implement the latest interface IP standards in their SoCs and want to take advantage of 25 percent lower power consumption or a 30 percent performance improvement offered by TSMC's 20SoC process compared to TSMC's 28-nm process. The DesignWare IP portfolio is designed to achieve high yield by meeting the requirements of advanced manufacturing design, such as adhering to double patterning layout rules.

"TSMC and Synopsys have a long history of collaboration on leading-edge process technology migration, delivering high-quality, proven IP that helps our mutual customers speed their time to volume production," said Suk Lee, TSMC senior director, design infrastructure marketing division. "The availability of Synopsys' high-quality IP portfolio for our 20SoC customers provides a low-risk path to implementing proven IP while reducing SoC power consumption."

Image: TSMC 20SoC silicon results for DesignWare PHY IP: Robust eye diagrams with excellent margin: https://www.synopsys.com/content/dam/synopsys/company/press-room/pr-tsmc20-silicon-results.jpg

As designs migrate to smaller process nodes, such as 20-nm and 16-nm FinFET, the technology challenges to extend Moore's Law become increasingly complex. TSMC has implemented double patterning mask technology on its 20SoC process utilizing two photo masks, each with half of a pattern, to enable printing of images below the node's minimum spacing design rules. Synopsys' development of DesignWare IP at 20-nm focused on minimizing yield and manufacturability issues while adhering to the standards' specifications, as well as TSMC's advanced layout and design rules for manufacturability with double patterning technology.

"As the leading provider of physical IP with more than 80 test chip tape-outs in 20- and 28-nm, Synopsys is focused on developing IP in the most advanced process nodes to help designers take full advantage of the processes speed and power characteristics while implementing high-quality, proven IP," said John Koeter, vice president of marketing for IP and systems at Synopsys. "By offering a broad portfolio of IP for the 20-nm process, Synopsys enables designers to more easily meet their goals of creating differentiated products with less risk and faster time to volume production, while also reducing the risks associated with moving to the 16-nm FinFET process."

Availability

The Synopsys DesignWare USB 2.0 PHY, USB 3.0 PHY, DDR4 multiPHY, PCI Express 2.0 PHY, and MIPI D-PHY for the TSMC 20SoC process are available now.

About DesignWare IP

Synopsys is a leading provider of high-quality, silicon-proven IP solutions for SoC designs. The broad DesignWare IP portfolio includes complete interface IP solutions consisting of controllers, PHY and verification IP for widely used protocols, analog IP, embedded memories, logic libraries, processor cores and subsystems. To support software development and hardware/software integration of the IP, Synopsys offers drivers, transaction-level models, and prototypes for many of its IP products. Synopsys' HAPS® FPGA-Based Prototyping Solution enables validation of the IP and the SoC in the system context. Synopsys' Virtualizer™ virtual

prototyping tool set allows developers to start the development of software for the IP or the entire SoC significantly earlier compared to traditional methods. With a robust IP development methodology, extensive investment in quality, IP prototyping, software development and comprehensive technical support, Synopsys enables designers to accelerate time-to-market and reduce integration risk. For more information on DesignWare IP, visit http://www.synopsys.com/designware.

About Synopsys

Synopsys, Inc. (Nasdaq:SNPS) accelerates innovation in the global electronics market. As a leader in electronic design automation (EDA) and semiconductor IP, Synopsys delivers software, IP and services to help engineers address their design, verification, system and manufacturing challenges. Since 1986, engineers around the world have been using Synopsys technology to design and create billions of chips and systems. Learn more at www.synopsys.com.

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