Synopsys Demonstrates Industry's First SuperSpeed USB Inter-chip (SSIC) Interoperability

Successful SSIC Interoperability Reduces Integration Risk and Speeds Time-to-Market for Mobile and Wireless Designs

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Highlights:

- Synopsys demonstrates industry's first SSIC interoperability at Intel Developer Forum 2013,September 10-12 in San Francisco, Calif.
- Demonstration shows DesignWare USB 3.0 IP for SSIC transferring data to and from an Intel SSIC development platform
- Implementing SSIC reduces chip-to-chip power consumption by up to 80 percent compared to conventional USB 3.0 technology for mobile and wireless devices
- SSIC chip-to-chip interconnect can re-use existing USB 3.0 software and drivers to save engineering years of effort
- Successful interoperability demonstration validates the robustness of the DesignWare USB 3.0 IP for SSIC, ensures that the IP functions in real-world applications and accelerates the development of SSIC-based designs

Synopsys, Inc. (Nasdaq:SNPS), a global leader providing software, IP and services used to accelerate innovation in chips and electronic systems, today announced the industry's first SuperSpeed USB Inter-chip (SSIC) interoperability demonstration. The demonstration shows the successful interoperability between Synopsys' DesignWare® USB 3.0 IP for SSIC and Intel Corporation's SSIC development platform, and is on display at the Intel Developer Forum 2013. Developed to reduce power consumption for mobile application processors and wireless chipsets, the SSIC specification from the USB 3.0 Promoter Group defines a low-power, on PCB, chip-to-chip interconnect that can re-use existing USB 3.0 software and drivers. With this successful demonstration, the companies validate the quality and interoperability of Synopsys' DesignWare® USB 3.0 IP for SSIC, giving system-on-chip (SoC) designers confidence in the reliability of their designs that utilize the IP.

"The SSIC specification leverages the low-power capabilities of the MIPI M-PHY while maintaining the high performance of USB 3.0 software and hardware," said Jeff Ravencraft, USB-IF President and COO. "When implementing SSIC functionality, which incorporates USB 3.0 controller IP and a MIPI M-PHY, designers can reuse their existing software drivers and benefit from their familiarity with the USB standard. Successful interoperability demonstrations from IP vendors like Synopsys help drive the evolution of USB and SSIC technology."

As consumers demand longer battery life for their mobile and wireless products, system architects are increasingly looking to new standard interfaces such as SSIC to reduce power consumption. The SSIC standard reduces chip-to-chip power consumption by up to 80 percent over conventional USB 3.0 technology for power-sensitive applications.

"With more than 3,000 USB IP design wins, Synopsys is focused on collaboration with key companies such as Intel to ensure that our IP is interoperable and functions as expected," said John Koeter, vice president of marketing for IP and systems at Synopsys. "Electronic product consumers continue to demand more functionality and longer battery life. DesignWare USB 3.0 IP for SSIC enables system architects building mobile and wireless connectivity devices to maximize power savings in their SoCs and end products."

Availability & Resources

The DesignWare USB 3.0 IP for SSIC is available now.
Additional information on Synopsys USB 3.0 SSIC IP is available:

- Article: Transitioning from USB 2.0 HSIC to USB 3.0 SSIC
- Video: Industry First: USB 3.0 SSIC Host and Device with MIPI M-PHY Demonstration
- USB Blog: To USB or Not To USB

About DesignWare IP

Synopsys is a leading provider of high-quality, silicon-proven IP solutions for SoC designs. The broad DesignWare IP portfolio includes complete interface IP solutions consisting of controllers, PHY and verification IP for widely used protocols, analog IP, embedded memories, logic libraries, processor cores and subsystems. To support software development and

hardware/software integration of the IP, Synopsys offers drivers, transaction-level models, and prototypes for many of its IP products. Synopsys' HAPS® FPGA-Based Prototyping Solution enables validation of the IP and the SoC in the system context. Synopsys' Virtualizer™ virtual prototyping tool set allows developers to start the development of software for the IP or the entire SoC significantly earlier compared to traditional methods. With a robust IP development methodology, extensive investment in quality, IP prototyping, software development and comprehensive technical support, Synopsys enables designers to accelerate time-to-market and reduce integration risk. For more information on DesignWare IP, visit https://www.synopsys.com/designware.

About Synopsys

Synopsys, Inc. (Nasdaq:SNPS) accelerates innovation in the global electronics market. As a leader in electronic design automation (EDA) and semiconductor IP, Synopsys delivers software, IP and services to help engineers address their design, verification, system and manufacturing challenges. Since 1986, engineers around the world have been using Synopsys technology to design and create billions of chips and systems. Learn more at www.synopsys.com.

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