Synopsys Announces DesignWare STAR Hierarchical System to Accelerate Silicon Testing of SoCs

Significantly Reduces Test Integration Time and Improves Test QoR for Hierarchical SoCs

MOUNTAIN VIEW, Calif., Sept. 9, 2013 /PRNewswire/ --

Highlights:

- Increase design and design-for-test (DFT) productivity with automatic test integration and validation of system-on-chip (SoC), including analog/mixed-signal IP, digital logic blocks, memory and interface IP
- Optimize test time and power consumption with dynamic parallel and serial test scheduling
- Re-use IP- and logic block-level test patterns at the SoC level, saving development time and effort
- Reduce test logic area and signal routing with streamlined hierarchical network based on IEEE test standards and managed by a modular server controller for all IP and logic blocks
- Reduce test development time by weeks with hierarchical access of IP and logic blocks
- Part of Synopsys' complete solution of test products, which includes DesignWare STAR Memory System, DFTMAX and TetraMAX

(Photo: http://photos.prnewswire.com/prnh/20130909/AQ75607)

Synopsys, Inc. (Nasdaq: SNPS), a global leader providing software, IP and services used to accelerate innovation in chips and electronic systems, today announced availability of its DesignWare® STAR Hierarchical System, an automated hierarchical test solution for efficiently testing SoCs, including analog/mixed-signal IP, digital logic blocks, memory and interface IP. The STAR Hierarchical System significantly reduces test integration time by automatically creating a hierarchical network based on IEEE test standards (IEEE 1500, IEEE 1149.1, P1687) that is managed by a modular server to access and control the test resources in the entire SoC. It improves test quality of results (QoR), including optimizing test time and power through flexible test scheduling.

"STMicroelectronics uses a variety of IP blocks in which test interfaces may differ, making it extremely challenging and time-consuming to integrate and test all of the IP at the SoC level," said Roberto Mattiuzzo, SoC Test and Diagnosis Group Manager at STMicroelectronics' Central CAD and Design Solutions. "Synopsys' DesignWare STAR Hierarchical System automates IP test integration in the SoC and enables the re-use of IP-level test patterns at the SoC level, cutting weeks off the design *and* the design-for-test cyclesand contributing to our getting products to market quickly. The solution also supports the upcoming standards for accessing embedded SoC DFT structures, allowing us to meet the requirements for board-level test."

The STAR Hierarchical System creates user-configurable IEEE 1500 interfaces in RTL for each IP and logic block in the SoC and integrates them with a top-level control module or server while maintaining a standard interface at every design hierarchy level. For designs with multiple levels of hierarchies, the solution offers a modular server in the desired hierarchy, instead of a single top-level server, to achieve test closure at the design hierarchy while minimizing the top-level signal routes. By utilizing existing, broadly adopted IEEE test standards, the STAR Hierarchical System enables easy integration of the SoC test resources, allowing global design teams working on different areas of the SoC to work more efficiently. The automatic creation of a streamlined hierarchical network and unified standard test interfaces, controlled by a central or modular server, improves area and signal routing and reduces test integration time by weeks. Additionally, the STAR Hierarchical System ports IP-level test patterns to the SoC level, leveraging the IEEE 1500 network for IP access, which eliminates the need to regenerate patterns and alleviates the capacity bottlenecks posed by large SoCs. Achieving test closure at the IP level and at all design hierarchy levels, as well as increased controllability and observability at the periphery of the IP and logic blocks, significantly improves test QoR for large SoCs.

"As designs continue to increase in size and use of more IP becomes essential, it is difficult to complete testing of large SoCs within the desired schedule and cost using traditional full-chip methodologies," said Dr. Yervant Zorian, fellow and chief architect at Synopsys. "Synopsys' new STAR Hierarchical System leverages IP-level and logic block-level test to efficiently test SoCs, enabling engineering teams to cut their test integration time to a matter of days and get their designs to market faster with lower design and test costs."

The STAR Hierarchical System gives designers the flexibility to schedule individual IP and logic blocks for parallel or serial testing to optimize time and power consumption during test. This flexible test scheduling can significantly reduce test time, especially for designs with limited I/Os. The solution provides automatic test equipment (ATE)-based and interactive board-based silicon debug and diagnostics to enable faster production ramp-up. The STAR Hierarchical System leverages IP debug test modes and enables diagnostics control and access from the SoC level. Additionally, it helps improve SoC yield by enabling

e-fuse programming through the server for calibration and trimming of analog/mixed-signal IP. The STAR Hierarchical System is compliant with the proposed IEEE standard P1687, which allows reuse of embedded test instruments for system-level debug.

All future Synopsys DesignWare analog and mixed-signal IP, such as USB, DDR and PCIe, will be delivered ready-to-use with the STAR Hierarchical System, which will enable designers to automatically create IEEE 1500 interfaces, integrate IP test structures on an SoC and use hierarchical testing. The DesignWare STAR Hierarchical System, along with the DesignWare STAR Memory System for embedded and external memory test, DFTMAX™ compression, TetraMAX™ ATPG solution, DesignWare IP with built-in self-test (BIST), Yield Explorer® design-centric yield analysis system and Camelot™ CAD navigation, provides designers and test engineers with a complete SoC test solution that increases test productivity, reduces overall test cost and improves test QoR.

"As the leading supplier of interface, analog and memory IP, Synopsys knows how pervasive IP is in large SoC designs and recognizes the difficulty of effectively testing these designs on a tight schedule and budget," said John Koeter, vice president of marketing for IP and systems at Synopsys. "Synopsys delivers DesignWare IP that is ready to use with the STAR Hierarchical System so that our customers can efficiently integrate and test Synopsys IP at the SoC level, which enables them to achieve faster design closure and improved test QoR."

Availability and Resources

The DesignWare STAR Hierarchical System is available now, and STAR Hierarchical System users will share their experiences at the 21st Annual Synopsys Test Special Interest Group meeting in Anaheim, California on September 9, 2013. Learn more about Synopsys' test solutions:

- Visit Synopsys at the International Test Conference (ITC) in Anaheim, California on September 10-12, 2013
- https://www.synopsys.com/SHS

About DesignWare IP

Synopsys is a leading provider of high-quality, silicon-proven IP solutions for SoC designs. The broad DesignWare IP portfolio includes complete interface IP solutions consisting of controllers, PHY and verification IP for widely used protocols, analog IP, embedded memories, logic libraries, processor cores and subsystems. To support software development and hardware/software integration of the IP, Synopsys offers drivers, transaction-level models, and prototypes for many of its IP products. Synopsys' HAPS® FPGA-Based Prototyping Solution enables validation of the IP and the SoC in the system context. Synopsys' Virtualizer virtual prototyping toolset allows developers to start the development of software for the IP or the entire SoC significantly earlier compared to traditional methods. With a robust IP development methodology, extensive investment in quality, IP prototyping, software development and comprehensive technical support, Synopsys enables designers to accelerate time-to-market and reduce integration risk. For more information on DesignWare IP, visit: https://www.synopsys.com/designware.

About Synopsys

Synopsys, Inc. (Nasdaq: SNPS) accelerates innovation in the global electronics market. As a leader in electronic design automation (EDA) and semiconductor IP, Synopsys delivers software, IP and services to help engineers address their design, verification, system and manufacturing challenges. Since 1986, engineers around the world have been using Synopsys technology to design and create billions of chips and systems. Learn more at www.synopsys.com.

Editorial Contacts:
Monica Marmie
Synopsys, Inc.
650-584-2890
monical@synopsys.com

Stephen Brennan
MCA, Inc.
650-968-8900, ext.114
sbrennan@mcapr.com

SOURCE Synopsys, Inc.