Synopsys Announces DFTMAX Ultra to Significantly Reduce Silicon Test Costs

Customers Realizing Up to 3x Higher Compression with Fewer Test Pins

MOUNTAIN VIEW, Calif., Sept. 9, 2013 /PRNewswire/ -- Synopsys, Inc. (Nasdaq: SNPS), a global leader providing software, IP and services used to accelerate innovation in chips and electronic systems, today announced its DFTMAX™ Ultra product, part of Synopsys' synthesis-based test solution, that significantly reduces silicon test cost. Embedded in Design Compiler® RTL synthesis and incorporating recently unveiled test technology, DFTMAX Ultra delivers up to 3x higher compression, enables testing of several die in parallel and utilizes the maximum performance of tester equipment to minimize silicon test time. To meet the need to increase quality and further reduce test cost without adversely impacting design goals and schedules, designers are deploying DFTMAX Ultra and realizing its benefits. Several users will share their experiences on both DFTMAX Ultra and the newly announced DesignWare® STAR Hierarchical System at the 21st Annual Synopsys Test Special Interest Group meeting in Anaheim, California on September 9, 2013.

"We always strive for highest level of reliability in our products; however this sometimes comes with a time penalty," said Realtek's vice president and spokesman, Jessy Chen. "DFTMAX Ultra reduces our test costs and time by a factor of three through high compression and the ability to run scan chains as fast as our testers operate. It is also very simple to deploy within our existing implementation flow and will help speed delivery of future designs."

Synopsys' DFTMAX Ultra contains recently developed technology that efficiently streams compressed test data in and out of the design-for-test (DFT) circuitry, significantly lowering the amount of data required to achieve high manufacturing test quality of silicon parts. The tool-generated architecture requires fewer test pins and enables silicon parts to operate at higher frequencies while in test mode. As a result, engineers can test more die in parallel and reduce the time required to test each die. For superior quality of results and faster turnaround time, design teams use DFTMAX Ultra together with the Synopsys Galaxy™ Implementation Platform suite of tools, concurrently optimizing and performing intelligent tradeoffs between speed, area, power, test and yield.

"We pioneered synthesis-based test and introduced DFTMAX compression in 2005. Together with TetraMAX ATPG, it has enabled designers to reduce their test costs while improving product quality," said Antun Domic, senior vice president and general manager of Synopsys' Implementation Group. "DFTMAX Ultra is our latest synthesis-based test innovation for design teams to meet even lower test cost and higher quality goals while adhering to tighter design schedules."

About Synopsys

Synopsys, Inc. (Nasdaq: SNPS) accelerates innovation in the global electronics market. As a leader in electronic design automation (EDA) and semiconductor IP, Synopsys delivers software, IP and services to help engineers address their design, verification, system and manufacturing challenges. Since 1986, engineers around the world have been using Synopsys technology to design and create billions of chips and systems. Learn more at http://www.synopsys.com.

Editorial Contacts:
Sheryl Gulizia
Synopsys, Inc.
650-584-4249
sgulizia@synopsys.com

Lisa Gillette-Martin
MCA, Inc.
650-968-8900 ext. 115
lgmartin@mcapr.com

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