Synopsys Launches DesignWare HDMI 2.0 TX/RX Controller and PHY IP for Ultra High-Definition Multimedia Experience

Full Support for New HDMI 2.0 Specification Provides Flickerless 4K x 2K Resolution for HDTVs

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Highlights:

- New DesignWare HDMI 2.0 IP provides 18 Gbps aggregate bandwidth in deep color mode to support ultra high-definition 4K x 2K resolution at 60 Hz frame rate
- Support for all HDMI 2.0 specification features, including YCbCr 4:2:0 color space, TMDS scrambling to reduce EMI and CEC 2.0 for advanced remote control units
- Robust analog front end supports 100+ foot long cables with 5-V tolerant I/Os
- Complete set of software drivers for Linux platform can reduce designers' software development effort from weeks to hours
- 28-nm PHY architecture offers 33 percent lower power and 25 percent smaller area compared to previous generation

Synopsys, Inc. (Nasdaq:SNPS), a global leader providing software, IP and services used to accelerate innovation in chips and electronic systems, today launched its DesignWare® HDMI 2.0 TX/RX IP solutions, including controller, PHY, and example Linux drivers to reduce designers' integration risk and time-to-market. With aggregate bandwidth of up to 18 Gbps, the DesignWare HDMI 2.0 IP enables 4K x 2K (4400 vertical pixels x 2250 horizontal pixels) resolution at a 60 Hz frame rate in deep color mode to provide a flickerless, ultra high-definition (UHD) viewing experience. The IP's ability to scramble transition-minimized differential signaling (TMDS) data above 3.4 Gbps adds to the high-quality viewing experience by minimizing the electromagnetic interference (EMI) that occurs in 8b/10b coded data streams. In addition, its robust analog front end supports pre-emphasis and adaptive equalization for excellent signal integrity across cables lengths of greater than 100 feet.

"We selected Synopsys' HDMI IP solution due to the company's strong mixed-signal and system-level expertise in the multimedia domain," said Michael Mo, senior director of business development at Amlogic. "Synopsys' early readiness with HDMI 2.0 has helped us incorporate the specification's advanced features into our 4K HDTV SoC. As a trusted IP vendor, Synopsys provided us with a high-quality product and expert technical support so we could focus resources on other aspects of our chip."

Image: Near-end eye diagram of Synopsys DesignWare HDMI 2.0 TX PHY in 28 nm with wide margin: http://www.synopsys.com/IP/InterfaceIP/HDMI%20Solutions/PublishingImages/pr-hdmi-figure.jpg

The DesignWare HDMI 2.0 IP solution offers a modular, flexible design that is optimized for area, power, pin count and gate count to reduce die size and bill-of-material (BOM) costs in HDTV system-on-chips (SoCs). The solution's configurability enables designers to future-proof their HDTV SoCs by supporting functional updates in software. The 28-nanometer (nm) HDMI 2.0 PHY offers 33 percent lower active and leakage power consumption than the previous generation to help comply with Energy Star requirements. In addition, the single PLL architecture and optimized I/O ring reduce silicon area by 25 percent compared to the previous generation. The HDMI 2.0 PHY can achieve 6 Gbps performance in a wirebond package, and the pin order can support a two-layer PCB board for BOM cost savings.

To assist in software development, Synopsys provides HDMI 2.0 drivers in the Linux kernel. The software drivers, which include high-bandwidth digital content protection (HDCP), extended display identification data (EDID) and consumer electronics control (CEC) functionality, can reduce designers' software development time from weeks to hours. For example, the CEC 2.0 driver supports the universal remote control standard, enabling consumers to control multiple home theater devices through a single remote control. The drivers may be used in Linux or Linux-based Android systems.

"Synopsys' HDMI 2.0 TX/RX solutions extend our leadership as a provider of high-quality IP for a wide range of multimedia consumer products," said John Koeter, vice president of marketing for IP and systems at Synopsys. "Our HDMI 2.0 IP has been architected to meet the performance requirements of ultra high-definition state-of-the-art home theater systems while providing design flexibility with support for future enhancements through software updates."

Availability

The DesignWare HDMI 2.0 RX/TX Controller and PHY IP are available now in 28-nm process nodes from multiple foundries.

About DesignWare IP

Synopsys is a leading provider of high-quality, silicon-proven IP solutions for SoC designs. The broad DesignWare IP portfolio includes complete interface IP solutions consisting of controllers, PHY and verification IP for widely used protocols, analog IP, embedded memories, logic libraries, processor cores and subsystems. To support software development and hardware/software integration of the IP, Synopsys offers drivers, transaction-level models, and prototypes for many of its IP products. Synopsys' HAPS® FPGA-Based Prototyping Solution enables validation of the IP and the SoC in the system context. Synopsys' Virtualizer™ virtual prototyping tool set allows developers to start the development of software for the IP or the entire SoC significantly earlier compared to traditional methods. With a robust IP development methodology, extensive investment in quality, IP prototyping, software development and comprehensive technical support, Synopsys enables designers to accelerate time-to-market and reduce integration risk. For more information on DesignWare IP, visit http://www.synopsys.com/designware.

About Synopsys

Synopsys, Inc. (Nasdaq:SNPS) accelerates innovation in the global electronics market. As a leader in electronic design automation (EDA) and semiconductor IP, Synopsys delivers software, IP and services to help engineers address their design, verification, system and manufacturing challenges. Since 1986, engineers around the world have been using Synopsys technology to design and create billions of chips and systems. Learn more at www.synopsys.com.

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