Samsung Widely Deploys Synopsys' Design Compiler Graphical for Mobile SoC Designs

Achieves Area and Power Reduction Critical to Success in the Mobile Market

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Highlights:

- Broad deployment of Design Compiler Graphical for Samsung Mobile SoCs
- Reduced routing congestion leads to 10 percent smaller area for highly congested blocks
- Minimal use of Low-Vt cells reduces leakage power while meeting frequency goals
- Congestion optimization and physical guidance to IC Compiler deliver superior results and faster design closure

Synopsys, Inc. (Nasdaq:SNPS), a global leader providing software, IP and services used to accelerate innovation in chips and electronic systems, today announced that Samsung Electronics has widely deployed the Design Compiler Graphical product, Synopsys' premium RTL Synthesis solution, to reduce power and area to deliver more competitive SoCs for the mobile market. Advanced technologies in Design Compiler Graphical, a key component of Synopsys' Galaxy™ Implementation Platform, including congestion optimization, advanced placement-based timing optimization and physical guidance to Synopsys' IC Compiler™ place and route solution, enable Samsung to achieve their challenging design goals and meet their schedule.

"Reducing area and power consumption while meeting performance goals is critical to the success of mobile SoCs targeted for today's mobile computing devices," said Kee Sup Kim, vice president of System LSI Infrastructure Design Center, Samsung Electronics. "We are using Design Compiler Graphical to help us deal with such technical challenges, and through the tight correlation with IC Compiler we achieve predictable implementation that meets our target design schedules to deliver value-added products for our customers."

Design Compiler Graphical addresses the needs of challenging designs at both advanced and established nodes. It includes technology shared with IC Compiler to consider physical effects, such as routing congestion and RC variation with metal layers during synthesis, to drive superior timing, area and power results. The advanced placement-based optimization of Design Compiler Graphical delivers 10 percent faster timing, minimizing the need for Low-Vt cells that have better timing but higher leakage power consumption. It passes physical guidance to IC Compiler, bringing synthesis timing and area results to within 5 percent of layout for a faster design closure. Design teams across all market segments are deploying Design Compiler Graphical and realizing its significant frequency, area, power and productivity benefits.

"Leaders in the mobile market, such as Samsung, rely on Design Compiler Graphical to get their products to market faster," said Antun Domic, senior vice president and general manager of Synopsys' Implementation Group. "Design Compiler Graphical's innovative synthesis technologies enable them to meet aggressive design and schedule goals that are essential to winning in this highly competitive space."

About Synopsys
Synopsys, Inc. (Nasdaq:SNPS) accelerates innovation in the global electronics market. As a leader in electronic design automation (EDA) and semiconductor IP, Synopsys delivers software, IP and services to help engineers address their design, verification, system and manufacturing challenges. Since 1986, engineers around the world have been using Synopsys technology to design and create billions of chips and systems. Learn more at www.synopsys.com.

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