Synopsys Launches Ultra-Low Power IP Subsystem for Sensors

Configurable Hardware and Software IP Solution Enables Rapid Integration of Sensor Functionality into SoCs

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Highlights:

- Integrated, pre-verified hardware and software IP subsystem consisting of a power- and area-efficient ARC 32-bit processor, digital and analog interfaces, hardware accelerators, software library of DSP functions and I/O software drivers
- Highly configurable with tightly integrated peripherals and dedicated hardware maximize sensor processing efficiency
- More than ten configurable hardware accelerators reduce memory footprint and decrease power consumption by a factor of 10 compared to equivalent discrete component implementations
- Extensive library of off-the-shelf software DSP functions, including mathematical, filtering, matrix/vector and decimation/interpolation, speeds application software development
- Enables implementations as small as 0.01mm^2, consuming less than 4uW/MHZ in a 28-nm process

Synopsys, Inc. (Nasdaq:SNPS), a global leader providing software, IP and services used to accelerate innovation in chips and electronic systems, today announced the availability of the DesignWare® Sensor IP Subsystem, a complete and integrated hardware and software solution for sensor control applications. The new IP subsystem is optimized to process data from digital and analog sensors, offloading the host processor and enabling more efficient processing of the sensor data with ultra-low power. The fully configurable subsystem consists of a DesignWare ARC® EM4 32-bit processor, digital interfaces, analog-to-digital data converters (ADCs), hardware accelerators, a comprehensive software library of DSP functions and software I/O drivers. The DesignWare Sensor IP Subsystem provides designers with a complete and pre-verified solution that meets the requirements of a broad range of applications such as smart sensors, sensor fusion and sensor hub.

Sensors are becoming ubiquitous. Many applications, such as the Internet of Things, automobiles, and mobile devices, increasingly rely on the ability to read and interpret environmental conditions such as pressure, temperature, motion, and proximity. By pre-integrating sensor-specific IP blocks with an efficient processor and software in a single subsystem, Synopsys gives designers a System-on-Chip [SoC]-ready sensor solution that can significantly reduce their design and integration effort, lower design risk and accelerate time-to-market.

"The total number of sensor units is estimated to grow from just under 10 billion in 2012 to nearly 30 billion in 2017," said Tony Massimini, chief of technology at Semico Research. "As more semiconductor suppliers integrate sensor interfaces into their SoCs, the use of sensor IP subsystems such as Synopsys' DesignWare Sensor IP Subsystem will significantly reduce their integration effort and cost."

Integrated Hardware

The DesignWare Sensor IP Subsystem features the power- and area-efficient DesignWare ARC EM4 32-bit processor core, which includes custom extensions and instructions that support application-specific hardware accelerators and tightly integrated peripherals. The subsystem includes multiple configurable GPIO, SPI and I2C digital interfaces for off-chip sensor connections as well as ARM® AMBA® AHB™ and APB™ protocol system interfaces to ease integration into the full SoC. The analog interfaces include low-power high-resolution ADCs that efficiently digitize sensor data for the processor. The sensor subsystem's HAPS® FPGA-based prototyping solution enables immediate software development and provides a scalable platform for rapid full system integration and validation. Synopsys also offers SoC integration services to help customers integrate the subsystem into their chip or customize it to meet their unique application requirements.

"As the technology leader in magnetic sensor ICs for the automotive market, it is critical that Allegro acquires high-quality IP from a trusted provider such as Synopsys," said Robert Fortin, director of sensors business unit at Allegro Microsystems, LLC. "Based on our experience, the DesignWare ARC 32-bit processor's combination of high performance, small area and low power provides key advantages for sensor design over alternative solutions."

Dedicated Software

The DesignWare Sensor IP Subsystem offers a rich library of DSP functions, including mathematical, complex math, filtering (FIR, IIR, correlation, etc.), matrix/vector and decimation/interpolation that help accelerate sensor application code development. In addition, peripheral software drivers are provided to ease integration of the I/O with the ARC EM4 processor, and host drivers are provided to interface the DesignWare Sensor IP Subsystem to the host processor.

The sensor-specific software functions can also be implemented in hardware to boost performance efficiency and reduce

memory footprint. An easy-to-use configuration tool in combination with sensor-specific architectural templates allow designers to quickly select options such as the DSP functions and digital interfaces required for their specific application, enabling a complete sensor subsystem to be configured in hours instead of weeks.

"The industry is seeing significant proliferation of sensor-enabled devices in homes, cars and on-the-go," said John Koeter, vice president of marketing for IP and systems at Synopsys. "These devices require integrated sensor SoCs that deliver high performance, small area and low power consumption. Synopsys' pre-verified, SoC-ready sensor subsystem provides designers with a higher level of hardware and software IP integration, enabling them to achieve their design goals faster and with significantly less risk."

Availability & Resources

The DesignWare Sensor IP Subsystem is targeted for availability in October 2013 to early adopters, with general availability planned for Q4 2013. For more information, please visit www.synopsys.com/sensorsubsystem.

About DesignWare IP
Synopsys is a leading provider of high-quality, silicon-proven IP solutions for SoC designs. The broad DesignWare IP portfolio includes complete interface IP solutions consisting of controllers, PHY and verification IP for widely used protocols, analog IP, embedded memories, logic libraries, processor cores and subsystems. To support software development and hardware/software integration of the IP, Synopsys offers drivers, transaction-level models, and prototypes for many of its IP products. Synopsys' HAPS FPGA-Based Prototyping Solution enables validation of the IP and the SoC in the system context. Synopsys' Virtualizer™ virtual prototyping tool set allows developers to start the development of software for the IP or the entire SoC significantly earlier compared to traditional methods. With a robust IP development methodology, extensive investment in quality, IP prototyping, software development and comprehensive technical support, Synopsys enables designers to accelerate time-to-market and reduce integration risk. For more information on DesignWare IP, visit: http://www.synopsys.com/designware.

About Synopsys
Synopsys, Inc. (Nasdaq:SNPS) accelerates innovation in the global electronics market. As a leader in electronic design automation (EDA) and semiconductor IP, Synopsys delivers software, IP and services to help engineers address their design, verification, system and manufacturing challenges. Since 1986, engineers around the world have been using Synopsys technology to design and create billions of chips and systems. Learn more at http://www.synopsys.com.

Forward-Looking Statements

This press release contains forward-looking statements within the meaning of Section 27A of the Securities Act of 1933 and Section 21E of the Securities Exchange Act of 1934, including statements regarding the expected availability of Synopsys' DesignWare Sensor IP Subsystem. These statements are based on current expectations and beliefs. Actual results could differ materially from those described by these statements due to risks and uncertainties including, but not limited to, unforeseen production or delivery delays, failure to perform as expected, product errors or defects and other risks as identified in Synopsys' filings with the Securities and Exchange Commission, including those described in the "Risk Factors" section of Synopsys' latest Quarterly Report on Form 10-Q.

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