Synopsys Announces Availability of Complete 28-nm Data Converter IP Portfolio

Latest Generation Reduces Power Consumption by up to 76 Percent and Area Use by up to 86 Percent for Mobile Communication SoCs

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Highlights:

- Complete portfolio of data converter IP includes high-speed and general-purpose ADCs and DACs
- New successive approximation register architecture for 12-bit ADCs supports conversion rates up to 320 MSPS
- 12-bit, 80 MSPS ADCs provide low 3.5 mW power consumption and 0.045 mm^2 area use for mobile communication applications

Synopsys, Inc. (Nasdaq:SNPS), a global leader providing software, IP and services used to accelerate innovation in chips and electronic systems, today announced the availability of its 28-nanometer (nm) data converter IP portfolio,which includes DesignWare® analog-to-digital converters (ADCs), digital-to-analog converters (DACs) and integrated PLLs. Implementing Synopsys' new data converter architecture in the 28-nm process node resulted in up to 76 percent reduction in power consumption and up to 86 percent reduction in area use, which reduces system costs for wireless networking and mobile communications system-on-chips (SoCs). Increasing Synopsys' 12-bit ADCs' performance to 320 megasamples per second (MSPS) enables greater flexibility for system definition in communications applications such as those enabled by LTE and WiFi 802.11ac protocols.

"As system architects move their designs to advanced process nodes, they are increasingly integrating analog interfaces directly into the main SoC instead of treating these functions as peripherals," said Richard Wawrzyniak, Senior Market Analyst, ASIC and SoC at Semico Research Corporation. "As a result, system architects need analog IP that is available in their required process nodes and meets their systems' area, performance and power supply voltage requirements. Analog IP providers like Synopsys are responding to this need by evolving their analog interfaces, and in particular their implementations of data converters, to take advantage of the high processing speeds and small area offered by advanced process nodes."

As designs continue to migrate to smaller process nodes such as 28 nm, designers need analog and mixed-signal IP area to scale along with the rest of the digital portion of the SoC. At the same time, overall system specifications are not relaxed to reflect the SoC's lower supply voltage, lower power and pin-count restrictions. To address these challenges, Synopsys has introduced the successive approximation register (SAR)-based architecture for its 12-bit high-speed ADCs, which offers parallel assembly options for improved area, lower power and architectural scalability. The ADCs currently offer conversion rates of up to 320 MSPS with architectural support for rates beyond 1 gigasample per second (GSPS). In addition, the 12-bit high-speed DACs increase conversion rates to 600 MSPS, a 50 percent increase in speed over the previous generation. Increased conversion rates allow for higher oversampling of the signal, which reduces filtering requirements at the output of the DACs and simplifies the circuit design.

"As the mobile industry moves to smaller SoC process nodes to meet consumer demand for higher performance, lower power consumption and smaller form factors, system architects are faced with a unique set of challenges that come with integrating 28-nanometer analog IP," said John Koeter, vice president of marketing for IP and systems at Synopsys. "Synopsys has invested significantly in designing and verifying our portfolio of 28-nanometer DesignWare IP to ensure interoperability and design robustness, and we have applied this extensive experience to our high-quality 28-nanometer data converter IP. With this portfolio of 28-nanometer analog IP solutions, Synopsys is enabling SoC designers to take advantage of the benefits of process scaling and reduce their communication designs' area and power consumption."

Availability

The DesignWare Data Converter IP is available now in the 28-nm process node.

About DesignWare IP

Synopsys is a leading provider of high-quality, silicon-proven IP solutions for SoC designs. The broad DesignWare IP portfolio includes complete interface IP solutions consisting of controllers, PHY and verification IP for widely used protocols, analog IP, embedded memories, logic libraries, processor cores and subsystems. To support software development and hardware/software integration of the IP, Synopsys offers drivers, transaction-level models and prototypes for many of its IP products. Synopsys' HAPS® FPGA-Based Prototyping

Solution enables validation of the IP and the SoC in the system context. Synopsys' Virtualizer™ virtual prototyping tool set allows developers to start the development of software for the IP or the entire SoC significantly earlier compared to traditional methods. With a robust IP development methodology, extensive investment in quality, IP prototyping, software development and comprehensive technical support, Synopsys enables designers to accelerate time-to-market and reduce integration risk. For more information on DesignWare IP, visit http://www.synopsys.com/designware.

About Synopsys

Synopsys, Inc. (Nasdaq:SNPS) accelerates innovation in the global electronics market. As a leader in electronic design automation (EDA) and semiconductor IP, Synopsys delivers software, IP and services to help engineers address their design, verification, system and manufacturing challenges. Since 1986, engineers around the world have been using Synopsys technology to design and create billions of chips and systems. Learn more at www.synopsys.com.

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