Synopsys and UMC Collaborate to Accelerate Development of UMC's 14-nm FinFET Process

Process Qualification Vehicle Tapeout Validates UMC 14-nm FinFET Process Using Synopsys DesignWare IP and StarRC Parasitic Extraction Tool

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Highlights

- First collaboration milestone speeds validation of IP and design correlation on UMC's 14-nm FinFET process
- Process qualification vehicle validates key process and IP test structures
- Tapeout helps accelerate adoption of the UMC FinFET process for faster and more power efficient system-on-chips (SoCs)

Synopsys, Inc. (Nasdaq:SNPS), a global leader providing software, IP and services used to accelerate innovation in chips and electronic systems, and United Microelectronics Corporation (NYSE:UMC;TWSE: 2303) ("UMC"), a leading global semiconductor foundry, today announced that the collaboration between the two companies has resulted in the successful tapeout of UMC's first process qualification vehicle in its 14-nanometer (nm) FinFET process utilizing Synopsys' DesignWare® Logic Library IP portfolio and StarRC™ parasitic extraction solution, a part of the Galaxy™ Implementation Platform.

Due to its performance, power, intra-die variability and lower retention voltage over the planar CMOS process, the FinFET process is gaining significant interest from designers. This process qualification vehicle will provide early silicon data, enabling UMC to tune its 14-nm FinFET process and Synopsys to refine its DesignWare IP portfolio for optimal power, performance and area. It also provides data to enable better correlation of the FinFET simulation models to the silicon results. This is the first milestone of an ongoing collaboration to validate UMC's 14-nm FinFET processes using DesignWare IP solutions.

"The successful tape-out of this qualification vehicle is a significant milestone for UMC," said Arthur Kuo, UMC vice president in charge of the company's corporate marketing division. "Our goal is to provide customers with a highly competitive FinFET technology solution that will help them maintain their products at the leading-edge. We selected Synopsys for this important collaboration based on their FinFET experience and expertise as well as their track record of developing high-quality DesignWare IP in the most advanced nodes. The results of this collaboration will yield significant benefits to the design community in the areas of power, performance and cost."

Synopsys' DesignWare Logic Library IP and StarRC Parasitic Extraction Tool

Synopsys' FinFET-ready DesignWare Logic Library IP portfolio consists of high-speed, high-density and low-power standard cell libraries that include multiple voltage threshold implementations and support multi-channel gate lengths to minimize leakage power. In addition, the available Power Optimization Kits (POKs) and Engineering Change Order (ECO) Kits deliver outstanding performance with low power and small area, meeting the speed and density requirements of advanced SoCs.

The StarRC parasitic extraction tool offers advanced extraction capabilities at 14 nm, based on precise 3-D modeling of the new parasitics found in FinFET devices. Due to its unique ability to describe the exact silicon profile of FinFET transistors, StarRC's embedded field solver generates highly accurate device model parasitics which enable 14-nm IP developers to optimize their designs for maximum performance and lowest power. Synopsys' Galaxy Implementation Platform also provides designers with a full suite of implementation tools that are FinFET-ready.

"Synopsys continues to lead the market in the development of IP and tools for FinFET technologies," said John Koeter, vice president of marketing for IP and systems at Synopsys. "Our collaboration with UMC further demonstrates our mutual commitment to delivering proven IP and tools that help designers lower integration risk and speed their time-to-volume production."

About UMC

UMC (NYSE: UMC, TWSE: 2303) is a leading global semiconductor foundry that provides advanced technology and manufacturing for applications spanning every major sector of the IC industry. UMC's robust foundry solutions allow chip designers to leverage the company's leading-edge processes, which include 28nm poly-SiON and gate-last High-K/Metal Gate technology, mixed signal/RFCMOS, and a wide range of specialty technologies. Production is supported through 10 wafer manufacturing facilities that include two advanced 300mm fabs; Fab 12A in Taiwan and Singapore-based Fab 12i. Fab 12A consists of Phases 1-4 which are in

production for customer products down to 28nm. Construction is underway for Phases 5&6, with future plans for Phases 7&8. The company employs over 13,000 people worldwide and has offices in Taiwan, Japan, China, Singapore, Europe, and the United States. UMC can be found on the web at http://www.umc.com.

About DesignWare IP

Synopsys is a leading provider of high-quality, silicon-proven IP solutions for SoC designs. The broad DesignWare IP portfolio includes complete interface IP solutions consisting of controllers, PHY and verification IP for widely used protocols, analog IP, embedded memories, logic libraries, processor cores and subsystems. To support software development and hardware/software integration of the IP, Synopsys offers drivers, transaction-level models, and prototypes for many of its IP products. Synopsys' HAPS® FPGA-Based Prototyping Solution enables validation of the IP and the SoC in the system context. Synopsys' Virtualizer virtual prototyping tool set allows developers to start the development of software for the IP or the entire SoC significantly earlier compared to traditional methods. With a robust IP development methodology, extensive investment in quality, IP prototyping, software development and comprehensive technical support, Synopsys enables designers to accelerate time-to-market and reduce integration risk. For more information on DesignWare IP, visit: http://www.synopsys.com/designware.

About Synopsys

Synopsys, Inc. (Nasdaq:SNPS) accelerates innovation in the global electronics market. As a leader in electronic design automation (EDA) and semiconductor IP, its software, IP and services help engineers address their design, verification, system and manufacturing challenges. Since 1986, engineers around the world have been using Synopsys technology to design and create billions of chips and systems. Learn more at http://www.synopsys.com.

Note from UMC Concerning Forward-Looking Statements

Some of the statements in the foregoing announcement are forward looking within the meaning of the U.S. Federal Securities laws, including statements about future outsourcing, wafer capacity, technologies, business relationships and market conditions. Investors are cautioned that actual events and results could differ materially from these statements as a result of a variety of factors, including conditions in the overall semiconductor market and economy; acceptance and demand for products from UMC; and technological and development risks. Further information concerning these risks is included in UMC's filings with the U.S. SEC, including on Form F-1, F-3, F-6 and 20-F, each as amended.

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