Synopsys Demonstrates Industry's First M-PCIe IP Interoperability

Comprehensive DesignWare IP Solution, Including Silicon-Proven MIPI M-PHY and M-PCIe Controller IP, Enables Early M-PCIe Adoption for Low-Power Designs

MOUNTAIN VIEW, Calif., June 25, 2013 /PRNewswire/ -- **Highlights:**

- Industry's first M-PCIe® IP interoperability demonstration, developed in conjunction with Intel, unveiled at PCI-SIG® Developers Conference 2013 taking place June 25 and 26, 2013 in Santa Clara, CA
- DesignWare® IP for M-PCIe, which includes the High-Speed Gear3 MIPI® M-PHY®, gives mobile device designers a low-power IP solution that reduces their time-to-market and integration risk
- Early support for M-PCIe extends Synopsys' technology leadership in PCI Express® and MIPI IP and accelerates designers' adoption of the new M-PCIe ECN

Synopsys, Inc. (Nasdaq:SNPS), a global leader providing software, IP and services used to accelerate innovation in chips and electronic systems, today announced the industry's first M-PCIe interoperability demonstration. The demonstration will be shown at the PCI-SIG Developers Conference 2013 and shows the successful interoperability between M-PCIe interfaces from Synopsys and Intel using M-PCIe-based switch and endpoint devices. M-PCIe is an engineering change notice (ECN) to the PCI Express (PCIe®) specification and enables designers to leverage their existing knowledge and software investments in PCI Express to reduce the power consumption of their systems-on-chips (SoCs) for low-power applications. Synopsys' M-PCIe solution, which includes silicon-proven DesignWare MIPI M-PHY technology and M-PCIe Controller IP, provides early support for the recently announced M-PCIe specification, enabling designers to accelerate development of their M-PCIe-based designs to hit critical market windows.

"Demonstrating M-PCIe interoperability with Synopsys is a significant milestone in accelerating the development of next-generation low-power mobile platforms," said Bob Gregory, ecosystem development manager, Intel Mobile and Communications Group. "The availability of robust IP, like Synopsys' M-PCIe IP solution, is an important step in integrating M-PCIe into the next generation of low power mobile devices. The IP provides designers with a proven platform for implementing the PCI Express protocol over the MIPI M-PHY."

The M-PCIe ECN to the PCI Express specification supports the low-power MIPI M-PHY by modifying the definition of the PCIe controller's physical layer. Synopsys has implemented this enhancement to its highly successful PCI Express controller IP, which has been used in over 750 designs, to work with its silicon-proven M-PHY and provide designers with a low-risk M-PCIe solution. Synopsys' implementation of the M-PCIe ECN includes the power saving features of the PCIe specification and adds support for asymmetric link widths and improved latency. The asymmetric links defined in the M-PCIe specification allow designers to provision different bandwidths in upstream and downstream directions for increased design flexibility and effective power allocation. The M-PCIe ECN also takes advantage of the M-PHY's specification for improved entry and exit latencies when going into and out of low-power modes, saving critical power for battery-powered devices.

"PCI-SIG developed the M-PCIe specification to enable PCIe architecture to operate over the M-PHY physical layer, extending the benefits of PCIe technology to the mobile and handheld industry," said Al Yanes, PCI-SIG President and Chairman. "Delivering PCIe technology across all platforms, from high-end servers and workstations to tablets and smartphones, enables designers to consolidate I/O technology, thereby reducing costs and time-to-market. As an active member of PCI-SIG, Synopsys is helping designers to adopt the latest PCI Express specifications by providing IP that allows them to integrate M-PCIe functionality in their SoCs."

The DesignWare Controller IP for M-PCIe is based on Synopsys' silicon-proven PCI Express controller IP, which has been extensively validated with multiple hardware platforms, PHYs and PCIe verification suites. Existing features and functions, such as application interfaces, embedded DMA engines, ARM® AMBA® AHB™/AXI™ bridges, support for multiple lanes (x1 to x16), and support for multiple data path widths, are proven in silicon and in wide customer use. In addition, DesignWare Controller IP for M-PCIe includes new selectable PHY technology, which allows one controller to support both PCI Express with a PIPE-interfaced PCI Express PHY and an RMMI interface for connection to Synopsys or third-party M-PHY. Because the DesignWare Controller IP for M-PCIe is based on the proven Synopsys PCI Express Controller IP, existing designs can be easily migrated into M-PCIe designs, while new designs benefit from the silicon-proven features.

Synopsys' M-PCIe solution incorporates the silicon-proven, High-Speed Gear3 DesignWare MIPI M-PHY. Designers can take advantage of the DesignWare MIPI M-PHY's support for the latest M-PHY specification (Version 3.00), Type-1, multiple gears (1,2,3), and multiple rates (A,B) to further reduce system power consumption for M-PCIe designs. Using a variety of high-speed and low-speed burst modes with power management modes, including stall, sleep, and hibernate with quick entry and exit capabilities, Synopsys' DesignWare MIPI M-PHY IP achieves required data rates while meeting the stringent power and area requirements of low-power devices.

"IP products supporting the MIPI M-PHY Version 3.00 specification helps designers prepare for the next generation of development while creating a robust ecosystem for low-power applications," said Joel Huloux, Chairman of MIPI Alliance. "Synopsys' MIPI M-PHY and controller IP for M-PCIe will help designers simplify their design process and reduce power for mobile device designs."

"We built upon our expertise and leadership in both PCI Express and MIPI IP to deploy the industry's first M-PCIe interoperability demonstration using M-PCIe interfaces from Synopsys and Intel," said John Koeter, vice president of marketing for IP and systems at Synopsys. "Our high-performance PCI Express controllers, which are the basis of our M-PCIe IP, have been used in more than 750 customer designs, and our MIPI M-PHY IP is used by many leading semiconductor vendors targeting the mobile industry. This track record of silicon-proven IP, coupled with the demonstration of DesignWare M-PCIe interoperability at the PCI-SIG Developers Conference, gives designers confidence that they can incorporate Synopsys' M-PCIe solution into their SoCs quickly and with minimal risk."

Availability

The DesignWare MIPI M-PHY is available now. The DesignWare Controller IP for M-PCIe is available now to early adopters.

About DesignWare IP

Synopsys is a leading provider of high-quality, silicon-proven IP solutions for SoC designs. The broad DesignWare IP portfolio includes complete interface IP solutions consisting of controllers, PHY and verification IP for widely used protocols, analog IP, embedded memories, logic libraries, processor cores and subsystems. To support software development and hardware/software integration of the IP, Synopsys offers drivers, transaction-level models, and prototypes for many of its IP products. Synopsys' HAPS® FPGA-Based Prototyping Solution enables validation of the IP and the SoC in the system context. Synopsys' Virtualizer™ virtual prototyping tool set allows developers to start the development of software for the IP or the entire SoC significantly earlier compared to traditional methods. With a robust IP development methodology, extensive investment in quality, IP prototyping, software development and comprehensive technical support, Synopsys enables designers to accelerate time-to-market and reduce integration risk. For more information on DesignWare IP, visit https://www.synopsys.com/designware.

About Synopsys

Synopsys, Inc. (Nasdaq:SNPS) accelerates innovation in the global electronics market. As a leader in electronic design automation (EDA) and semiconductor IP, its software, IP and services help engineers address their design, verification, system and manufacturing challenges. Since 1986, engineers around the world have been using Synopsys technology to design and create billions of chips and systems. Learn more at www.synopsys.com.

About PCI-SIG

PCI-SIG is the consortium that owns and manages PCI specifications as open industry standards. The organization defines industry standard I/O (input/output) specifications consistent with the needs of its members. Currently, PCI-SIG is comprised of nearly 800 industry-leading member companies. To join PCI-SIG, and for a list of the Board of Directors, visit www.pcisig.com.

About MIPI Alliance

MIPI® Alliance (MIPI) develops interface specifications for mobile and mobile-influenced industries. Founded in 2003, the organization has more than 220 member companies worldwide, 12 active working groups and has delivered more than 30 specifications within the mobile ecosystem in the last decade. Members of the organization include handset manufacturers, device OEMs, software providers, semiconductor companies, application processor developers, IP tool providers, test and test equipment companies, as well as camera, tablet and laptop manufacturers. For more information, please visit www.mipi.org.

PCI-SIG, PCI Express, M-PCIe and PCIe are all trademarks or registered trademarks of PCI-SIG.
MIPI and M-PHY are registered marks of MIPI Alliance.

Editorial Contacts:
Monica Marmie
Synopsys, Inc.
650-584-2890
monical@synopsys.com

Stephen Brennan
MCA, Inc.
650-968-8900, ext.114
sbrennan@mcapr.com

SOURCE Synopsys, Inc.