Synopsys Delivers 2X Speedup for Implementing and Verifying Functional ECOs

New Formality Ultra Extends Equivalency Checking to Accelerate Design Closure

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Highlights:

- New Synopsys Formality® Ultra solution cuts days of effort for each functional engineering change order (ECO)
- Includes advanced matching, visualization and fast verification technologies
- Customers reporting 2X speedup for implementing and verifying functional ECOs

Synopsys, Inc. (Nasdaq:SNPS), a global leader providing software, IP and services used to accelerate innovation in chips and electronic systems, today announced Formality Ultra, a new configuration of the Formality equivalency checking solution. Formality Ultra includes innovative matching and verification technologies to efficiently guide designers through the implementation of functional ECOs with minimal impact to the design and verify the correctness of the ECOs in minutes for multimillion instance designs. These new capabilities will help designers cut in half the time they spend implementing ECOs late in the design cycle and result in shorter, more predictable schedules.

Complex designs often undergo multiple functional ECOs late in the design process due to changing specifications and functional errors. Each ECO change can adversely impact schedule and predictability of design closure, which causes designers to invest days trying to minimize the impact of every change to the design. This process can add weeks in the late stages of the design cycle.

"With the new ECO capabilities in Formality Ultra, we can cut in half the time needed for implementing functional ECOs and shorten our design schedules," said Bruce Fishbein, vice president of NCD IC Engineering at Cavium Inc. "It will also enable us to implement more complex functional changes as ECOs rather than wait for the next derivative of the design. We are planning to deploy Formality Ultra on our next project."

The new Formality Ultra adds advanced matching techniques that visually highlight the mismatch between the RTL and netlist representations of a design, allowing designers to efficiently zoom in on the changes required to implement an ECO. In addition, a new multi-point verification technology very quickly checks multiple changes made to the design enabling designers to verify the correctness of their ECOs in a matter of minutes on multi-million instance designs.

"Designers worldwide rely on Formality's equivalency checking technology to verify their complex, high-frequency designs without sacrificing chip performance or design schedules," said Antun Domic, senior vice president and general manager of Synopsys' Implementation Group. "Formality Ultra extends this technology to address another key challenge they face – functional ECOs. It enables designers to significantly reduce the time and effort required to implement those ECOs, increase schedule predictability and close their designs on time."

About Synopsys

Synopsys, Inc. (Nasdaq: SNPS) accelerates innovation in the global electronics market. As a leader in electronic design automation (EDA) and semiconductor IP, its software, IP and services help engineers address their design, verification, system and manufacturing challenges. Since 1986, engineers around the world have been using Synopsys technology to design and create billions of chips and systems. Learn more at http://www.synopsys.com.

Editorial Contacts:
Sheryl Gulizia
Synopsys, Inc.
650-584-8635
sgulizia@synopsys.com

Lisa Gillette-Martin
MCA, Inc.
650-968-8900 ext. 115
lgmartin@mcapr.com

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