Synopsys Announces Design Kit Optimized for All SoC Processor Cores

DesignWare HPC Design Kit Yields Superior Performance, Power and Area for CPU, GPU and DSP Cores

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Highlights:

- One design kit for optimizing all processor cores on an SoC that includes an ultra-high density memory compiler and more than 125 new standard cells and memory instances
- Delivers up to 10 percent performance improvement on host CPU cores and up to 25 percent lower power with 10 percent area reduction on GPU cores such as the Imagination Technology PowerVR Series6 IP core
- Developed in close collaboration with key partners including Imagination Technologies, CEVA and VeriSilicon
- Implement your optimized processor cores in as little as four to six weeks with Synopsys *FastOpt* services

Synopsys, Inc. (Nasdaq:SNPS), a global leader providing software, IP and services used to accelerate innovation in chips and electronic systems, today announced an extension to its DesignWare® Duet Embedded Memory and Logic Library IP portfolio specifically designed to enable the optimized implementation of a broad range of processor cores. The new DesignWare HPC (High Performance Core) Design Kit contains a suite of high-speed and high-density memory instances and standard cell libraries that allow system-on-chip (SoC) designers to optimize their on-chip CPU, GPU and DSP IP cores for maximum speed, smallest area or lowest power – or to achieve an optimum balance of the three for their specific application.

"Our work with Synopsys has resulted in significant improvements in the area and energy efficiency implementations of our IP cores utilizing Synopsys' memories and standard cell libraries," said Mark Dunn, executive vice-president of IMGworks SoC Design at Imagination Technologies. "Our most recent project was building a PowerVR™ Series6 GPU core using cells and memories from Synopsys' HPC Design Kit. We achieved an overall reduction of 25 percent in dynamic power as well as a 10 percent area savings, with some blocks achieving a 14 percent area improvement. We also created a tuned design flow that has delivered a 30 percent improvement in implementation turnaround time."

Synopsys' broad portfolio of DesignWare IP includes silicon-proven embedded memory compilers and standard cell libraries that support a range of foundries and processes from 180 to 28 nanometers (nm) and have shipped in more than three billion chips. The DesignWare Duet Package of Embedded Memories and Logic Libraries contains all the physical IP elements needed to implement a complete SoC including standard cells, SRAM compilers, register files, ROMs, datapath libraries and Power Optimization Kits (POKs). Options for overdrive/low- voltage process, voltage and temperature (PVT) corners, multi-channel cells, and memory built-in self-test (BIST) and repair are also available. The DesignWare HPC Design Kit adds performance-, power- and area-optimized standard cells and memory instances tuned for the special speed and density requirements of advanced CPU, GPU and DSP cores.

"The physical IP used for implementing processor cores has a tremendous impact on the achievable power, performance and area of the design," said Nianfeng Li, corporate vice president of design methodologies and program management at VeriSilicon. "When we consider all the factors that contribute to an optimized implementation, the DesignWare Duet Embedded Memories and Logic Libraries have been a primary contributor to the performance gains we realized on the recent hardening of a leading CPU core. The new DesignWare HPC Design Kit contains the specialty cells and SRAMs we need to achieve the highest possible performance on advanced processor cores while minimizing area and power consumption."

"DSPs are a fundamental component of every advanced electronic product, from smartphones and tablets to smart TVs and base stations, and each design has unique optimization requirements," said Eran Briman, vice president of marketing at CEVA, Inc. "In addition to extreme performance, designers rely on our DSP cores to consume as little power and occupy as little silicon area as possible. We look forward to continued collaboration with Synopsys in helping our mutual customers achieve their strict design goals."

The HPC Design Kit contains fast cache memory instances and performance-tuned flip-flops that enable speed improvement of up to 10 percent over the standard Duet package. To minimize dynamic and leakage power as well as die area, the new kit provides area-optimized and multi-bit flip-flops and an ultra-high-density two-port SRAM, delivering demonstrated reductions in area and power of up to 25 percent while maintaining processor performance.

Optimized design flow scripts and expert core optimization consulting, including *FastOpt* implementation services, are also available from Synopsys to help design teams achieve their processor and SoC design goals in the shortest possible time.

"Designers using any of Imagination's IP, including PowerVR graphics and video, MIPS processors and Ensigma communications processors, will ultimately be able to reap benefits from leveraging Synopsys' HPC Design Kit, thanks to their deep experience working with Imagination and delivering services to our customers over many years," added Mark Dunn of Imagination. "Through projects including our strategic collaboration with Synopsys, we're putting practical solutions in place to help our customers achieve performance-, power- and area-optimized designs utilizing our IP in the shortest time."

"Designers implementing processor cores must make tradeoffs in speed, power and area that will result in the best implementation for their specific application, and physical IP plays an important role in achieving that optimum design," said John Koeter, vice president of marketing for IP and systems at Synopsys. "We have worked closely with leading customers and IP partners that implement a broad range of processor cores to gain insight on how to achieve the absolute best results on their design and reflected that collective learning in the new DesignWare HPC Design Kit. In one package, designers now have access to the specialty cells and memories they need to optimize their CPU, GPU and DSP cores across the full speed, power and area spectrum."

Availability & Resources

The DesignWare HPC Design Kit will be available for leading 28-nm processes starting in July 2013.

Learn more about the DesignWare HPC Design Kit: http://www.synopsys.com/hpc-ip.

About DesignWare IP

Synopsys is a leading provider of high-quality, silicon-proven IP solutions for SoC designs. The broad DesignWare IP portfolio includes complete interface IP solutions consisting of controllers, PHY and verification IP for widely used protocols, analog IP, embedded memories, logic libraries, processor cores and subsystems. To support software development and hardware/software integration of the IP, Synopsys offers drivers, transaction-level models, and prototypes for many of its IP products. Synopsys' HAPS® FPGA-Based Prototyping Solution enables validation of the IP and the SoC in the system context. Synopsys' Virtualizer virtual prototyping tool set allows developers to start the development of software for the IP or the entire SoC significantly earlier compared to traditional methods. With a robust IP development methodology, extensive investment in quality, IP prototyping, software development and comprehensive technical support, Synopsys enables designers to accelerate time-to-market and reduce integration risk. For more information on DesignWare IP, visit: http://www.synopsys.com/designware.

About Synopsys

Synopsys, Inc. (Nasdaq:SNPS) accelerates innovation in the global electronics market. As a leader in electronic design automation (EDA) and semiconductor IP, its software, IP and services help engineers address their design, verification, system and manufacturing challenges. Since 1986, engineers around the world have been using Synopsys technology to design and create billions of chips and systems. Learn more at http://www.synopsys.com.

Forward-Looking Statements

This press release contains forward-looking statements within the meaning of Section 27A of the Securities Act of 1933 and Section 21E of the Securities Exchange Act of 1934, including statements regarding the expected availability and performance of Synopsys' DesignWare HPC Design Kit. These statements are based on current expectations and beliefs. Actual results could differ materially from those described by these statements due to risks and uncertainties including, but not limited to, unforeseen production or delivery delays, failure to perform as expected, product errors or defects and other risks as identified in Synopsys' filings with the Securities and Exchange Commission, including those described in the "Risk Factors" section of Synopsys' latest Quarterly Report on Form 10-Q.

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