# Synopsys Unveils New Synthesis-Based Test Technology Delivering Up to 3X Higher Compression

## Innovative Technology Includes Advances for Pin-Limited Test

MOUNTAIN VIEW, Calif., June 11, 2013 /PRNewswire/ -- Synopsys, Inc. (Nasdaq: SNPS), a global leader providing software, IP and services used to accelerate innovation in chips and electronic systems, today unveiled a new, innovative test technology to further reduce the cost of testing silicon devices by delivering up to 3x higher test compression and minimizing the time required to test each silicon die. The new technology also uses fewer pins and higher-frequency on-chip design-for-test (DFT) circuitry, enabling design teams to test several die in parallel and use the maximum performance of their tester equipment to achieve additional reduction in test time and cost. Embedded in Synopsys' Design Compiler® RTL synthesis and TetraMAX® ATPG solutions, the new test technology delivers faster test time and higher test quality without adversely impacting design goals and schedules.

"Our initial review of Synopsys' new test technology shows it can achieve up to three times higher compression compared to existing solutions," said Roberto Mattiuzzo, SoC test and diagnosis manager at STMicroelectronics' Central CAD and Design Solutions. "The technology can be deployed on a variety of design styles with any number of test pins and supports high-speed test clocks. It is well aligned with our ever-increasing requirements to lower the cost and raise the quality of test for our silicon products using our current and ready-for-production fabrication process."

Engineers are increasingly testing silicon parts in parallel and at faster frequencies while adding more tests. Synopsys' new synthesis-based test technology uses an innovative method to efficiently stream compressed test data in and out of the DFT circuitry, significantly lowering the amount of data required to achieve high test quality. This method requires fewer test pins and enables silicon parts to operate at higher frequencies while in test mode. As a result, more die can be tested in parallel, and the time required to test each die is further reduced. To deliver superior quality of results and faster turnaround time, design teams implement the DFT for the new technology with the Synopsys Galaxy™ Implementation Platform suite of tools, concurrently balancing design constraints by performing intelligent tradeoffs between speed, area, power, test and yield.

"Designers across different industry segments have widely adopted and relied on our DFTMAX compression to reduce cost, improve quality and get their products to market on time," said Antun Domic, senior vice president and general manager of Synopsys' Implementation Group. "Our latest synthesis-based test innovation will help them meet more stringent test cost and quality goals within tighter design schedules."

**About Synopsys**

Synopsys, Inc. (Nasdaq: SNPS) accelerates innovation in the global electronics market. As a leader in electronic design automation (EDA) and semiconductor IP, its software, IP and services help engineers address their design, verification, system and manufacturing challenges. Since 1986, engineers around the world have been using Synopsys technology to design and create billions of chips and systems. Learn more at http://www.synopsys.com.

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