TSMC Certifies Synopsys' Digital and Custom Solutions for 16-nm FinFET Process

V0.1 Certification Based on Collaboration over Key Foundational Technologies

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Highlights:

- Collaboration on Synopsys' StarRC™ and QuickCap® tools for 3-D parasitic extraction
- Solution deployed by early adopters of TSMC FinFET process
- Includes Synopsys' IC Compiler™, IC Validator, StarRC, PrimeTime®, Laker® Layout, Galaxy Custom Designer®, FineSIM™ and CustomSIM™ products and solutions

Synopsys, Inc. (Nasdaq: SNPS), a global leader providing software, IP and services used to accelerate innovation in chips and electronic systems, today announced that TSMC has certified a comprehensive list of custom and digital design tools from Synopsys for 16-nm FinFET process Design Rule Manual (DRM) and SPICE V0.1. TSMC's certification is built on early collaboration for extraction and modeling of 3-D parasitics in FinFET devices and extends to full-line design implementation solutions. Certification includes all the relevant 16-nm technology routing rules, verification runsets, extraction rundecks and Interoperable Process Design Kits (iPDK). Results from the collaboration are enabling early adopters of the TSMC 16-nm process to realize the potential of FinFET technology to develop faster and more power-efficient designs.

The certified Synopsys Galaxy Implementation Platform features comprehensive support for TSMC 16-nm V0.1 design rules. TSMC has certified a full suite of Synopsys implementation tools that are FinFET-ready. This includes:

- IC Compiler: Innovative double patterning technology (DPT)-aware placement and routing provides optimal area and performance results that can be reliably decomposed during manufacturing
- IC Validator: DRC and DPT rule compliance check verifying FinFET parameters including fin boundary rules and expanding dummy cells.
- PrimeTime: Accurate delay calculation and timing analysis to include impact of double patterning
- StarRC: Extraction of parasitics impacted by the 3-D structure of FinFET devices and relevant extensions to Interconnect Technology Format (ITF)
- FineSim and CustomSIM: Correct and accurate functionality with the FinFET BSIM-CMG models
- Custom Designer and Laker Layout: Improved productivity through connectivity-assisted editing with support for 16-nm constraints to help manage design-rule complexity

"Our collaboration with TSMC highlights our goal to enable transparent adoption of FinFET technology for our mutual customers," said Bijan Kiani, vice president of Product Marketing, Design & Manufacturing Products at Synopsys. "To achieve this goal we engaged with TSMC on a comprehensive and deep collaboration spanning digital as well as custom implementation and verification tools."

"Certification of Synopsys tools for our 16-nanometer process is a critical milestone in the rollout of our FinFET technology," said Suk Lee, TSMC Senior Director, Design Infrastructure Marketing Division. "Our FinFET collaboration started earlier than at previous nodes due to the complexity involved in modeling the 3-D FinFET devices. This certification helps early adopters get trusted access to our advanced process and accelerates deployment of FinFET technology."

About Synopsys

Synopsys, Inc. (Nasdaq:SNPS) accelerates innovation in the global electronics market. As a leader in electronic design automation (EDA) and semiconductor IP, its software, IP and services help engineers address their design, verification, system and manufacturing challenges. Since 1986, engineers around the world have been using Synopsys technology to design and create billions of chips and systems. Learn more at http://www.synopsys.com.

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