Synopsys Plans Full Slate of Special Events at DAC 2013

Industry Experts, Customers and Partners to Provide Insight into the Latest Technology Advancements, Trends and Capabilities Leveraging Synopsys' Innovative Solutions

MOUNTAIN VIEW, Calif., May 23, 2013 /PRNewswire/ -- Synopsys, Inc. (Nasdaq: SNPS), a global leader providing software, IP and services used to accelerate innovation in chips and electronic systems, will offer a variety of special events at the Design Automation Conference, June 2-6, in Austin, Texas. The events will feature speakers from leading semiconductor makers, IP providers and foundries, as well as Synopsys. These technology experts will describe the best practices, tools and methodologies they're using to continue accelerating the pace of innovation throughout the industry.

Synopsys DAC Events, Monday, June 3, 2013:

- **ARM-TSMC-Synopsys Breakfast: Optimizing Implementation of Performance- and Power-Balanced Processor Cores**
  7:15 a.m. - 8:45 a.m., Austin Hilton Hotel, 6th Floor, Grand Ballroom H
  This session will highlight the latest technologies in Synopsys' Design Compiler® Graphical and IC Compiler™ tools that you can use to efficiently optimize the implementation of processor cores to meet power and performance targets. You will learn about engineering trade-offs and best practices utilized to implement an ARM Cortex-A15 dual-core processor optimized first for performance, then power, and a Cortex-A7 quad-core processor optimized first for energy efficiency, then maximum speed.
- **AMS Luncheon: Advance Your Mixed-Signal Verification Techniques to the Next Level**
  11:30 a.m. - 1:30 p.m., Austin Hilton Hotel, 6th Floor, Grand Ballroom G
  From low power and reliability to mixed-signal verification and memory characterization, attendees will learn from experts in SoC, memories and IP how to further advance current AMS methodologies for performance and accuracy using the latest Synopsys AMS verification solutions.
- **IC Compiler Luncheon: The Many Faces of Advanced Technology**
  11:30 a.m. - 1:30 p.m., Austin Hilton Hotel, 6th Floor, Grand Ballroom H
  Designers are constantly looking for solutions to their most advanced design challenges. But "advanced" can mean different things to different people. At this luncheon, experts from foundry, processor, wireless and consumer electronics companies will share their successes in harnessing IC Compiler's technology advancements to address a range of cutting-edge design challenges.
- **Customer Insight Sessions: Success with Synopsys' Galaxy™ Implementation Platform**
  2:00 p.m. - 3:00 p.m.: YK Lee, Principal Engineer, Samsung
  3:00 p.m. - 4:00 p.m.: Michael V. Leuzze, Design Center Manager, LSI
  Austin Convention Center, Level 3, Room 10B
  These highly informative sessions will cover the latest design trends, challenges and solutions. Leading industry experts will present best practices and their success with Synopsys implementation products. In addition, they will share how they have accelerated innovation to meet their gigascale, gigahertz, low-power and advanced-geometry design challenges.
- **PrimeTime Special Interest Group (SIG) Dinner: Technology Panel – Advanced ECO Methodology**
  6:00 p.m. - 9:30 p.m., Brazos Hall, 204 E. 4th Street
  This event will feature a panel of leading experts in timing technology. Panelists from STMicroelectronics, Altera and Samsung will share their vision and experience on advanced engineering change order (ECO) methodologies that accelerate design closure on the most advanced technology nodes.

Synopsys DAC Events, Tuesday, June 4, 2013:

- **GLOBALFOUNDRIES-Synopsys Breakfast: Deploying 14XM FinFETs in Your Next Mobile SoC Design**
  7:15 a.m. - 8:45 a.m., Austin Hilton Hotel, 6th Floor, Grand Ballroom G
  Hear industry experts discuss the challenges and key design advantages of adopting FinFET technology and learn how GLOBALFOUNDRIES and Synopsys are collaborating to deliver a comprehensive EDA, IP and manufacturing-ready solution optimized for mobile SoC design using 14nm-XM FinFET technology.
- **Visionary Talk with Synopsys Chairman and co-CEO Aart de Geus Massive Innovation and Collaboration in the "GigaScale" Age!**
  9:15 a.m. – 9:30 a.m., Austin Convention Center, Ballroom ABC
  The semiconductor industry is on the bridge to a new world of complexity empowered by smaller dimensions, new transistor types, enormous IP reuse, and a focus on the potential of electronic systems. Dr. de Geus will provide an overview of the enormous amount of recent innovation and collaboration that will enable "Moore's Law plus, plus" for yet another decade.
- **Customer Insight Sessions: Success with Synopsys' Galaxy™ Implementation Platform**

10:00 a.m. - 11:00 a.m.: Martin Foltin, Master Technologist, HP
2:00 p.m. - 3:00 p.m.: Tim Whitfield, Director of Engineering, ARM
Austin Convention Center, Level 3, Room 10B
These highly informative sessions will cover the latest design trends, challenges and solutions. Leading industry experts will present best practices and their success with Synopsys implementation products. In addition, they will share how they have accelerated innovation to meet their gigascale, gigahertz, low-power and advanced-geometry design challenges.

- **Custom Design Luncheon: Addressing Custom Design Challenges with Laker**
  11:30 a.m. – 1:30 p.m., Austin Hilton Hotel, 6th Floor, Grand Ballroom G
  From coping with complex 20-nm design rules to handling high voltages and currents with ever-smaller layout geometries, custom layout challenges are once again becoming a top concern for many design teams. Laker® tool users present their views on key issues confronting custom designers, and discuss how they are using Laker to layout their most advanced ICs.
- **Verification Luncheon: SoC Leaders Verify with Synopsys**
  11:45 a.m. - 1:45 p.m., Austin Hilton Hotel, 6th Floor, Grand Ballroom H
  Given the complexity of today's SoC designs, incremental tool improvements will not be sufficient to deliver the necessary order-of-magnitude boost to verification productivity. What's needed are true innovations in verification. Industry experts will discuss what's driving SoC complexity and share how they're achieving success.
- **IPL Alliance Dinner: iPDKs: A Thriving PDK Standard**
  6:00 p.m. - 7:30 p.m., Austin Hilton Hotel, 6th Floor, Grand Ballroom G
  As of 2012, 4 of the top 5 semiconductor pure-play foundries have joined the IPL Alliance, and all the top 5 foundries have provided customers with iPDKs. At the 7th Annual IPL Luncheon, IPL Alliance presenters will highlight the benefits of the iPDK standards and their experiences in developing and deploying foundry iPDKs. The IPL Alliance will also present an update on current and future projects as well as collaboration with other industry initiatives.

Synopsys at DAC 2013

Visit Synopsys at Booth #947 to learn about the newest solutions available to help designers accelerate their innovations. In addition to special events, Synopsys will offer demonstrations of its custom design, Design Compiler, IC Compiler and functional verification solutions. Synopsys will also feature the following technology exhibits: HAPS® Family of FPGA-Based Prototyping Solutions; and Functional Verification: A Comprehensive Solution for Addressing Rising SoC Challenges. For more information on all of Synopsys' activities at DAC, visit www.synopsys.com/DAC.

Media Registration Information

Seating is limited at Synopsys' special events at DAC. Registration is required. Members of the media interested in attending Synopsys' special events or requiring more information should email inquiries to Diane Hayward at dhayward@mcapr.com.

About Synopsys

Synopsys, Inc. (Nasdaq: SNPS) accelerates innovation in the global electronics market. As a leader in electronic design automation (EDA) and semiconductor IP, its software, IP and services help engineers address their design, verification, system and manufacturing challenges. Since 1986, engineers around the world have been using Synopsys technology to design and create billions of chips and systems. Learn more at www.synopsys.com.

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