Synopsys DesignWare IP for PCI Express 3.0 Passes First PCI-SIG PCIe 3.0 Compliance Workshop

Silicon-Proven PCI Express 3.0 Digital Controller and PHY IP Solution Lowers Integration Risk for SoC Designs

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Highlights:

- Synopsys' DesignWare digital controller and PHY IP for PCI Express 3.0 passed PCI-SIG®'s three required Gold Tests and completed interoperability with more than the requisite 80 percent of the devices at the workshop
- Complete PCI Express 3.0 solution, including PHY, controller and verification IP, reduces integration risk while minimizing time-to-market
- PCI Express 3.0 controllers, optimized for high performance, low latency and low gate counts, support x1 to x16 lanes and ARM® AMBA® AXI4™, AXI3™, and AHB™ interconnect
- Energy-efficient PCI Express 3.0 PHY offers high-performance analog front-end for robust signal integrity and is available in leading 28-nanometer (nm) process nodes

Synopsys, Inc. (Nasdaq:SNPS), a global leader providing software, IP and services used to accelerate innovation in chips and electronic systems, today announced that its DesignWare® PHY and digital controller IP for the PCI-SIG® PCI Express® 3.0 is the first complete solution from a single vendor to pass compliance testing at the first PCI-SIG compliance workshop for PCI Express 3.0. The PCI Express 3.0 specification increases the operating rate to 8 gigatransfers per second (GT/s), effectively doubling the bandwidth over PCI Express 2.0 to address the high-performance requirements of data center, storage and networking applications. To achieve compliance, the DesignWare PHY and controller IP passed PCI-SIG's three required Gold Tests: the electrical tests, the Protocol Test Card (PTC) and the PCIeCV software tests. In addition, the DesignWare PHY and controller IP demonstrated interoperability with more than 80 percent of the devices at the workshop, exceeding interoperability requirements. By providing a complete and compliant IP solution for PCI Express 3.0, Synopsys enables designers to immediately incorporate the high-performance PCI Express 3.0 interface into their system-on-chips (SoCs) with less risk and improved time-to-market, while helping to ensure product interoperability.

"As the leader in application-intelligent 10 Gigabit Ethernet network interface software and hardware, we rely on Synopsys to provide us with high-performance PCI Express IP that helps us differentiate our products in the market," said Andre Chartand, vice president of engineering at Solarflare. "Synopsys' high-quality IP for PCI Express 3.0, including the scalable I/O virtualization support necessary for our cloud and software defined networking offerings, as well as the company's superior technical support, were instrumental in the silicon success of our next-generation SFN7000 design."

"Teledyne LeCroy has collaborated with Synopsys through multiple generations of DesignWare PCI Express IP to ensure interoperability and standards compliance," said John Wiedemeier, PCI Express product marketing manager at Teledyne LeCroy. "Synopsys' ongoing commitment to performing extensive compliance testing to the latest specifications, including their recent success at the PCI-SIG Compliance Workshop, significantly lowers the barrier for designers to incorporate high speed PCIe interfaces into their chips."

The complete DesignWare IP for PCI Express solution includes PHYs, controllers and verification IP. DesignWare IP for PCI Express has been used in more than 750 designs, with more than 80 for PCI Express 3.0. The full-featured, high-performance digital controller IP for PCI Express 3.0 provides an optional interface to connect to ARM AMBA AXI4, AMBA AXI3 or AMBA AHB on-chip interconnect using the DesignWare IP for PCI Express Bridge, which allows designers to easily add PCI Express 3.0 functionality to their SoCs. The PHYs substantially exceed the PCI Express electrical specifications in key performance areas such as jitter margin and receive sensitivity, which enable a more reliable PCI Express link.

"As an active member of the PCI-SIG since 2003, Synopsys understands the importance of contributing to the PCI Express specification working groups and participating in compliance testing as part of the ecosystem enablement," said Al Yanes, PCI-SIG president. "Synopsys' compliance to the latest version of the PCI Express 3.0 specification helps ensure compatibility among products incorporating PCI Express while facilitating the widespread adoption of PCI Express 3.0."

"To maintain our leadership in PCI Express IP, we make continuous investments in new product features and conduct rigorous compliance testing to ensure our IP meets the latest specifications," said John Koeter, vice president of marketing for IP and systems at Synopsys. "We have moved aggressively to align our PCI Express roadmap with the industry's needs by providing PCI Express 3.0 support since the 0.5 version of the specification. Early availability enabled our customers to meet their aggressive time-to-market requirements. Achieving this latest compliance milestone gives designers confidence that they can incorporate a complete PCI Express solution into their SoCs that will meet their full performance and interoperability

requirements."

Availability

The DesignWare Controller for PCI Express 3.0 is available now. The DesignWare PHY IP for PCI Express 3.0 is available now in multiple 28-nm technology nodes.

About DesignWare IP

Synopsys is a leading provider of high-quality, silicon-proven IP solutions for SoC designs. The broad DesignWare IP portfolio includes complete interface IP solutions consisting of controllers, PHY and verification IP for widely used protocols, analog IP, embedded memories, logic libraries, processor cores and subsystems. To support software development and hardware/software integration of the IP, Synopsys offers drivers, transaction-level models, and prototypes for many of its IP products. Synopsys' HAPS® FPGA-Based Prototyping Solution enables validation of the IP and the SoC in the system context. Synopsys' Virtualizer™ virtual prototyping tool set allows developers to start the development of software for the IP or the entire SoC significantly earlier compared to traditional methods. With a robust IP development methodology, extensive investment in quality, IP prototyping, software development and comprehensive technical support, Synopsys enables designers to accelerate time-to-market and reduce integration risk. For more information on DesignWare IP, visit https://www.synopsys.com/designware.

About Synopsys

Synopsys, Inc. (Nasdaq:SNPS) accelerates innovation in the global electronics market. As a leader in electronic design automation (EDA) and semiconductor IP, its software, IP and services help engineers address their design, verification, system and manufacturing challenges. Since 1986, engineers around the world have been using Synopsys technology to design and create billions of chips and systems. Learn more at www.synopsys.com.

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