HiSilicon Technologies Tapes Out 50+ Million Instance ARM Processor-based SoC Using Synopsys IC Compiler

Latest IC Compiler Innovations Meet Performance Targets on Time

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Highlights:

- HiSilicon taped out a 50+ million instance ARM® Cortex™-A15 processor-based system-on-a-chip (SoC)
- Improved clock speed by 100 MHz through IC Compiler™ multisource clock tree synthesis (CTS) technology
- Reduced leakage power by 10% to 20% on power-sensitive blocks with IC Compiler final-stage leakage recovery
- Accelerated timing closure with Design Compiler® Graphical physical guidance and IC Compiler transparent interface optimization
- Enabled faster ECO closure with PrimeTime® signoff-driven ECO guidance

Synopsys, Inc. (Nasdaq: SNPS), a global leader providing software, IP and services used to accelerate innovation in chips and electronic systems, today announced that HiSilicon Technologies, a leading end-to-end chipset solution provider for telecom network, wireless terminal and digital media, has taped out a 50+ million instance ARM® Cortex™-A15 processor based system-on-chip (SoC) using Synopsys' IC Compiler, a key component of Synopsys' Galaxy™ Implementation Platform. The latest technology innovations in IC Compiler, including improved clock tree synthesis (CTS) and faster top-level closure, were key to meeting performance and schedule on this gigascale SoC.

"At HiSilicon, we continually innovate to deliver complex SoC solutions that are well differentiated in terms of performance and functionality," said Teresa He, President, HiSilicon Technologies Co., Ltd. "We have long recognized the importance of working with leading-edge partners like Synopsys to enable us to achieve our design objectives. On this multi-million instance SoC tapeout, we used the latest technologies in the Galaxy Implementation Platform to develop a correlated and predictable design closure flow that met our aggressive performance targets for on-time delivery."

The 50+ million instance HiSilicon SoC targeting the wireless chipset market contains multiple ARM Cortex-A15 processors, peripheral logic and memories. It was implemented hierarchically and fabricated on a TSMC 28HPM process using TSMC standard cell libraries and fast cache instance memories. The high operating frequency meant that clock skew and on-chip-variation (OCV) tolerance targets were very low. At the same time, due to the tight schedule, a correlated and convergent flow for faster design closure was a key implementation requirement. HiSilicon leveraged the Synopsys High Performance Core (HPC) methodology, which utilizes several key technologies from the Galaxy Implementation Platform, on this successful tapeout, including:

- Design Compiler Graphical physical guidance to enable correlation within 3 percent of IC Compiler
- IC Compiler variation-aware multisource clock tree synthesis technology to achieve approximately 40 percent reduction in skew and 100 MHz improvement in operating clock speed
- IC Compiler transparent interface optimization (TIO) to accelerate top-level timing closure for the processor clusters
- IC Compiler final-stage leakage recovery for 10 to 20 percent leakage power reduction on power-sensitive blocks
- PrimeTime signoff-driven ECO guidance with IC Compiler for faster ECO closure

"HiSilicon Technologies has a growing reputation as a leading chipset solution provider for the wireless and networking markets," said Antun Domic, senior vice president and general manager, Synopsys Implementation Group. "Our partnership with HiSilicon Technologies has benefitted both companies by shaping unique technologies in IC Compiler which have contributed to its growing use in the physical design space."

About Synopsys

Synopsys, Inc. (Nasdaq:SNPS) accelerates innovation in the global electronics market. As a leader in electronic design automation (EDA) and semiconductor IP, its software, IP and services help engineers address their design, verification, system and manufacturing challenges. Since 1986, engineers around the world have been using Synopsys technology to design and create billions of chips and systems. Learn more at www.synopsys.com.

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