Latest Release of Synopsys IC Compiler Introduces New Technologies to Further Speed Design Closure

New Innovations Address ECO Closure, High-speed Design and Emerging Process Nodes

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Highlights:

- Innovative new technologies including minimum physical impact ECO and fully incremental In-Design physical verification speed up design closure for all process nodes
- Concurrent clock and data optimization enables faster timing closure on high-speed designs
- Provides full, color-ready place-and-route and tapeout-proven FinFET support for emerging process nodes

Synopsys, Inc. (Nasdaq: SNPS), a global leader providing software, IP and services used to accelerate innovation in chips and electronic systems, today announced the availability of the 2013.03 release of its IC Compiler™ software, a key component of Synopsys' Galaxy™ Implementation Platform. Adding to the market-leading foundation of design closure technologies already available in IC Compiler, this latest release features innovations to speed design as well as enables the latest process nodes. New features include advanced optimizations to enable high-speed design, efficient implementation of final-stage engineering change orders (ECO) and fully color-ready, tapeout-proven support for the emerging FinFET-based silicon processes.

"Mellanox Technologies designs, builds and manufactures the world's leading interconnect solutions for connecting datacenter server and storage platforms. As such, we require the best IC design tools in the market," said Evelyn Landman, vice president of backend engineering at Mellanox Technologies. "Synopsys' IC Compiler helps us to achieve our engineering goals, and we look forward to utilizing its new design closure capabilities that can further advance the IC design process."

The IC Compiler 2013.03 release includes powerful new features to deliver even faster design closure. One important new capability is the application of final-stage ECOs to close the design. IC Compiler, working hand-in-hand with Synopsys' PrimeTime® signoff solution, provides a highly efficient ECO solution rooted in dual principles: first, ensuring that very few ECOs are required after the optimization steps; and second, applying the ECOs surgically with minimal layout perturbation. In this flow, PrimeTime provides signoff-accurate ECO guidance, implemented using the new minimum physical impact ECO capability, which greatly reduces layout perturbation by reusing wires and minimizing device displacement. Combined with a fully automatic, incremental In-Design physical verification capability, IC Compiler provides a significant reduction in turnaround time for ECO closure.

Another area that continues to receive increased attention in advanced chips is clock design. With high-speed designs, the clock distribution network can be a significant contributor to total power. While clock gating is an established technique to minimize clock network power, meeting clock gate timing requirements can be a challenge. Additionally, aggressive clock speeds call for innovative new solutions that combine datapath optimization with clock cycle adjustment. The 2013.03 IC Compiler release enables high-speed clock design by performing clock estimation during placement to drive physical- and timing-aware clock gating concurrently with clock and data optimization to achieve the target frequency faster.

IC Compiler 2013.03 delivers these improvements while expanding support for new silicon technology. Since its introduction, IC Compiler has consistently led the way for emerging process node enablement. The previous release of IC Compiler rolled out support for the 20-nm node, which brought many new design challenges including double patterning (DPT). In this latest release, Synopsys' close collaboration with foundries and early adopters to deliver a fully color-ready, tapeout-proven solution for emerging FinFET-based designs fortifies IC Compiler's strong track record of enabling emerging nodes.

"We continue to deliver technology innovations that target pressing customer needs," said Antun Domic, senior vice president and general manager, Synopsys Implementation Group. "Companies like Mellanox Technologies who are doing advanced design with strong time–to-market demands will benefit from new technologies for faster ECO closure and high-speed clock design. Combined with our strong focus on emerging node technology, these advanced capabilities reinforce IC Compiler's position as the preferred implementation choice across the IC design community."

About Synopsys

Synopsys, Inc. (Nasdaq:SNPS) accelerates innovation in the global electronics market. As a leader in electronic design automation (EDA) and semiconductor IP, its software, IP and services help engineers address their design, verification, system and manufacturing challenges. Since 1986, engineers around the world have been using Synopsys technology to design and create billions of chips and systems. Learn more at www.synopsys.com.

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