Synopsys Unveils Embedded Vision Development System

Reduces Development Time for Power- and Performance-Optimized Application-Specific Processors from Months to Weeks

MOUNTAIN VIEW, Calif., April 25, 2013 /PRNewswire/ --

Highlights

- Accelerate development of application-specific processors for embedded vision applications by taking advantage of Synopsys® Processor Designer ™ tool set, processor examples and pre-verified design methodologies
- Explore new processor architectures tailored to embedded vision requirements in hours instead of weeks
- Reduce system bring-up time by months with pre-validated embedded vision reference flows for Synopsys HAPS® FPGA-based prototypes

Synopsys, Inc. (Nasdaq:SNPS), a global leader providing software, IP and services used to accelerate innovation in chips and electronic systems, today announced the immediate availability of the Embedded Vision Development System, an integrated solution for the acceleration of the design of processors for embedded vision based on Synopsys' Processor Designer tool set and Synopsys' HAPS FPGA-based prototyping system. Application-specific instruction-set processors (ASIPs) are essential for meeting the power efficiency requirements of system-on-chips (SoCs) supporting high-performance embedded vision applications, such as advanced driver assistance systems (ADAS), augmented reality (AR), robotics, surveillance and gesture control. The new Synopsys Embedded Vision Development System enables designers to rapidly explore and tune processor architectures for the optimal combination of power and speed, and quickly implement the design on a HAPS FPGA-based prototype.

"Embedded vision enables designers to add visual intelligence to systems, making them safer, smarter and more responsive," said Jeff Bier, founder of the Embedded Vision Alliance (www.Embedded-Vision.com). "But embedded vision is processing-intensive and most applications demand extreme cost- and energy-efficiency while also requiring programmability to accommodate new algorithms and new functions over time. Custom processors like those enabled by the Synopsys Embedded Vision Development System often yield the best mix of performance, efficiency and flexibility. I applaud Synopsys for recognizing and supporting the growing importance of embedded vision."

The Embedded Vision Development System includes pre-verified design examples to help designers quickly implement an ASIP optimized to meet their specific SoC objectives for power consumption and performance. It provides a ready-to-use, modifiable base processor including a full C/C++ compiler, which supports all functions provided by the OpenCV library. The execution of the compiled code with the automatically-generated instruction-set simulator (ISS) is easy to profile, clearly identifying performance-intensive parts of the application, which can be accelerated by changes in the processor architecture, including memory access, register configuration and instruction set. Unlike configurable processors that rely on a fixed pipeline and register structure, this methodology removes limitations from achieving the most power- and performance-optimized custom architecture for their application. Using the automatically generated software tools, designers easily recompile and simulate the C/C++ program until they achieve their design goals.

Processor Designer generates optimized RTL of the ASIP, which can easily be downloaded into a HAPS FPGA-based prototyping system. Designers save implementation effort with an easy-to-use flow from RTL generation to instantiation in the HAPS system, using the same RTL from design through validation. HAPS prototypes allow the design team adopting the application-specific processor to integrate other digital IP into the SoC design and connect the prototype with real-world I/O such as cameras and memory to validate the hardware-software integration. Running more than 100x faster than a cycle-accurate ISS-based model, the combination of Processor Designer and HAPS in the new integrated design and prototyping system provides a highly-efficient way to refine and validate ASIP architectures from project to project.

"Many types of electronic devices require designers to develop custom processors to meet unique performance goals most efficiently, such as the processing of large amounts of visual data in embedded vision systems," said John Koeter, vice president of marketing for IP and systems at Synopsys. "The Synopsys Embedded Vision Development System, based on Processor Designer and a linkage to HAPS FPGA-based prototyping, saves months of engineering effort by combining software and hardware tools that enable designers to analytically arrive at the best processor implementation for their specific application, then quickly prototype the entire SoC to complete the hardware/software integration."

Availability & Resources

The Embedded Vision Development System is immediately available from Synopsys.

-

- Learn more about the Embedded Vision Development Systemhttp://www.synopsys.com/PD

Embedded Vision Development System at the Embedded Vision Summit 2013

Synopsys will be demonstrating the Embedded Vision Development System at the Embedded Vision Summit in San Jose, California on April 25, 2013. For more information: http://www.embedded-vision.com/embedded-vision-summit.

About Synopsys

Synopsys, Inc. (Nasdaq:SNPS) accelerates innovation in the global electronics market. As a leader in electronic design automation (EDA) and semiconductor IP, its software, IP and services help engineers address their design, verification, system and manufacturing challenges. Since 1986, engineers around the world have been using Synopsys technology to design and create billions of chips and systems. Learn more at http://www.synopsys.com.

Editorial Contacts:
Tess Cahayag
Synopsys, Inc.
650-584-5446
maritess@synopsys.com

Stephen Brennan
MCA, Inc.
650-968-8900, ext.114
sbrennan@mcapr.com

SOURCE Synopsys, Inc.