Fujitsu Semiconductor ASIC Design for 2G/3G/4G Baseband Processor in Volume Production with Synopsys 28-nm MIPI M-PHY

DesignWare MIPI IP Enables Silicon and Commercial Success of High-Performance, Low-Power Baseband Processor

MOUNTAIN VIEW, Calif., April 9, 2013 /PRNewswire/ --

Highlights:

- Fujitsu Semiconductor achieved silicon success and compliance with the latest DigRFv4 standard using Synopsys' DesignWare® MIPI M-PHY IP
- DesignWare MIPI M-PHY's proven interoperability between DigRFv4 interface on the baseband side and Fujitsu Semiconductor's radio frequency integrated circuit (RFIC) helped accelerate delivery of customer's ASIC to market, enabling quick product ramp
- Fujitsu Semiconductor achieved aggressive low power consumption goals for their customer's ASIC design for multi-band mobile application

Synopsys, Inc. (Nasdaq:SNPS), a global leader providing software, IP and services used to accelerate innovation in chips and electronic systems, today announced that Fujitsu Semiconductor Limited is successfully shipping a 2G/3G/4G baseband processor using Synopsys' DesignWare DigRFv4 M-PHY and DigRF 3G PHY IP. Fujitsu Semiconductor selected Synopsys' silicon-proven IP to mitigate project schedule risks and help ensure the long-term interoperability of their ASIC design customer's system-on-chip (SoC) with Fujitsu Semiconductor's RFIC products. Integrating DesignWare IP allowed Fujitsu Semiconductor to deliver an efficient, low-power and cost-effective solution.

"Our customer's next-generation mobile devices required low-power, high-bandwidth connectivity, so we needed a reliable IP solution in the required process technology that was compliant with MIPI standard specifications," said Daisuke Yamazaki, manager, design department, wireless solution division at Fujitsu Semiconductor. "Integrating Synopsys' DesignWare DigRFv4 M-PHY and DigRF 3G PHY IP helped ensure the successful silicon tapeout and production ramp of mobile SoCs targeting 2G/3G/4G speeds with high data rates and low power consumption."

Fujitsu Semiconductor's ASIC design services customer needed to launch its mobile platform quickly with a low-power 28-nanometer (nm) 2G/3G/4G baseband product supporting multimode, multi-band LTE, UMTS, and EDGE mobile handsets with full support for all global FDD and TDD bands. Since both the target 28-nm process technology and the MIPI specifications were being finalized in parallel with the integration of Synopsys' M-PHY into the ASIC, Synopsys and Fujitsu Semiconductor worked closely to maintain clear and consistent communication throughout the product development cycle to ensure a successful tapeout. The engineering teams were able to identify and address differences between the DigRFv4 and DigRF 3G standard specifications, keeping the project schedule on track.

"Synopsys understands the importance of providing companies like Fujitsu Semiconductor with high-quality IP that enables them to reduce integration risk and focus internal resources on other critical parts of the design," said John Koeter, vice president of marketing for IP and systems at Synopsys. "Fujitsu Semiconductor's successful integration of the 28-nanometer DesignWare M-PHY demonstrates our commitment to delivering silicon-proven IP so that our customers can deliver innovative products to the market faster."

Availability

The DesignWare M-PHY supporting multiple protocols, including DigRFv4, and the DigRF 3G PHY are available for multiple process nodes now.

About DesignWare IP

Synopsys is a leading provider of high-quality, silicon-proven IP solutions for SoC designs. The broad DesignWare IP portfolio includes complete interface IP solutions consisting of controllers, PHY and verification IP for widely used protocols, analog IP, embedded memories, logic libraries, processor cores and subsystems. To support software development and hardware/software integration of the IP, Synopsys offers drivers, transaction-level models, and prototypes for many of its IP products. Synopsys' HAPS® FPGA-Based Prototyping Solution enables validation of the IP and the SoC in the system context. Synopsys' Virtualizer™ virtual prototyping tool set allows developers to start the development of software for the IP or the entire SoC significantly earlier compared to traditional methods. With a robust IP development methodology, extensive

investment in quality, IP prototyping, software development and comprehensive technical support, Synopsys enables designers to accelerate time-to-market and reduce integration risk. For more information on DesignWare IP, visit http://www.synopsys.com/designware.

About Synopsys

Synopsys, Inc. (Nasdaq:SNPS) accelerates innovation in the global electronics market. As a leader in electronic design automation (EDA) and semiconductor IP, its software, IP and services help engineers address their design, verification, system and manufacturing challenges. Since 1986, engineers around the world have been using Synopsys technology to design and create billions of chips and systems. Learn more at www.synopsys.com.

Editorial Contacts:
Monica Marmie
Synopsys, Inc.
650-584-2890
monical@synopsys.com

Stephen Brennan
MCA, Inc.
650-968-8900, ext.114
sbrennan@mcapr.com

SOURCE Synopsys, Inc.