Avnet ASIC Israel Switches to Synopsys to Accelerate SoC Design

HERZELIA, Israel, March 19, 2013 – Synopsys, Inc. (Nasdaq: SNPS), a global leader providing software, IP and services used to accelerate innovation in chips and electronic systems, today announced that Avnet ASIC Israel (AAI), a provider of system-on-chip (SoC) design, layout and manufacturing services has chosen Synopsys as its electronic design automation (EDA) provider for SoC design. AAI replaced its existing flow with Synopsys' Galaxy™ Implementation platform and Discovery™ Verification Platform, and adopted DesignWare® IP. With Synopsys' unified digital and custom implementation platform, integrated portfolio of functional, analog/mixed-signal, debug, formal, low-power and hardware-assisted verification tools and silicon-proven IP, Avnet can leverage the powerful combination of its SoC design services and Synopsys' advanced methodologies to provide ASIC companies in Israel with faster time-to-market.

"By switching to Synopsys, AAI can now provide the services and solutions that will enable our customers to meet their power, performance, reliability and cost requirements as they transition to smaller process nodes," said Nadav Ben-Ezer, general manager of AAI. "Leveraging a state-of-the-art CAD platform, advanced methodologies, silicon-proven IPs, local support, Hebrew-speaking technologists and close collaboration between the design teams, our customers can reduce design risks and shorten time-to-market for their end products." Customers may also utilize AAI's additional turn-key services for testing, characterizing and qualifying their devices for mass production and to develop system-in-package (SIP) devices for maximum system miniaturization.

"Synopsys' implementation and verification platforms are the tools of choice for leading-edge SoC design," said Ehud Loewenstein, sales manager of Synopsys in Israel. "Our engagement with Avnet extends the deployment of Synopsys technology in Israel and enables Avnet's ASIC customers to benefit from the high quality of results and fast turnaround time that can be achieved with Synopsys tools and IP."

Accelerating Innovations in Advanced IC Design

The Galaxy Implementation Platform is a comprehensive solution for cell-based and custom IC implementation. Galaxy accepts design intent in industry standard formats and generates a production ready IC design in GDSII format. Galaxy RTL and Physical implementation products concurrently balance design constraints by performing intelligent tradeoffs between speed, area, power, test and yield. Galaxy Signoff engines accurately model complex physical interactions to help ensure signal and power integrity. Coherent algorithms for parasitic extraction and timing produce correlated results.

Delivering a New Level of Verification Excellence

The Discovery Verification Platform is an integrated portfolio of functional, AMS, debug, formal, low-power and hardware-assisted verification tools. Discovery provides high performance, high accuracy and efficient interactions among best-in-class technologies including mixed-HDL simulation, mixed-signal simulation, assertions, coverage, testbench automation, verification IP, formal analysis, unified debug, equivalence checking, acceleration, emulation and rapid prototyping. Discovery's components support industry standards including SystemVerilog, SystemC, VHDL, UPF, OpenVera, Verilog-A, Verilog-AMS, SPICE, and more.

About DesignWare IP

Synopsys is a leading provider of high-quality, silicon-proven IP solutions for SoC designs. The broad DesignWare IP portfolio includes complete interface IP solutions consisting of controllers, PHY and verification IP for widely used protocols, analog IP, embedded memories, logic libraries and configurable processor cores. To support software development and hardware/software integration of the IP, Synopsys offers drivers, transaction-level models, and prototypes for many of its IP products. Synopsys' HAPS FPGA-Based Prototyping Solution enables validation of the IP and the SoC in the system context. Synopsys' Virtualizer™ virtual prototyping tool set allows developers to start the development of software for the IP or the entire SoC significantly earlier compared to following traditional methods. With a robust IP development methodology, extensive investment in quality, IP prototyping, software development and comprehensive technical support, Synopsys enables designers to accelerate time-to-market and reduce integration risk. For more information on DesignWare IP, visit: http://www.synopsys.com/designware.

About Synopsys

Synopsys, Inc. (Nasdaq: SNPS) accelerates innovation in the global electronics market. As a leader in electronic design automation (EDA) and semiconductor IP, its software, IP and services help engineers address their design, verification, system and manufacturing challenges. Since 1986, engineers around the world have been using Synopsys technology to design and create billions of chips and systems. Learn more at http://www.synopsys.com.

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