Imagination Technologies Selects Synopsys as Advanced Verification Technology Partner

Multi-year Collaboration Results in Deployment of Synopsys' Advanced Formal Debug Technology for Verification of PowerVR Graphics Intellectual Property (IP) Cores

MOUNTAIN VIEW, Calif., Jan. 30, 2013 /PRNewswire/ -- Synopsys, Inc. (NASDAQ: SNPS), a global leader providing software, IP and services used to accelerate innovation in chips and electronic systems, today announced Imagination Technologies has deployed Synopsys' C–to-RTL formal consistency checking technology, named HECTOR, to verify its PowerVR family of semiconductor IP cores for graphics, video and display processing applications. Following a multi-year collaboration with Synopsys, Imagination Technologies is utilizing HECTOR to enhance its verification environment with the ability to verify and debug corner cases.

"Synopsys' HECTOR technology has enabled us to perform formal equivalence checking between system-level models and RTL over a range of complex PowerVR cores," said Martin Ashton, vice president of Imagination's PowerVR IP engineering group. "The HECTOR technology has allowed us to complete formal verification in minutes, where exhaustive techniques would have been impractical. As a result, HECTOR has enabled us to significantly improve the design verification capabilities within our PowerVR GPU team. We anticipate using HECTOR across all our IP design groups, while, thanks to our close and creative engagement with Synopsys' HECTOR R&D team, we continue to explore new applications of this exciting technology."

"With the increasing complexity of system-on-chips (SoCs), next-generation verification technologies are essential to more effectively manage SoC quality, schedule and cost," said Manoj Gandhi, senior vice president and general manager of the Synopsys Verification Group. "We are delighted to have such close R&D level collaborations with Imagination Technologies, a leading innovator in the industry, enabling us to deliver ground-breaking technologies that address growing verification challenges."

Multimedia applications involve complex algorithmic functional blocks requiring their behavior to be modeled in high-level languages such as C, and subsequently ensuring that the implemented RTL description is functionally equivalent. Conventional simulation-based verification of these design elements can be time-consuming and is likely to miss corner-case design bugs that would manifest only in the SoC where the IP core becomes embedded. With HECTOR, design teams are able to exhaustively verify all combinations of inputs and gain a high level of confidence in the quality of their IP blocks.

About Synopsys
Synopsys, Inc. (Nasdaq:SNPS) accelerates innovation in the global electronics market. As a leader in electronic design automation (EDA) and semiconductor IP, its software, IP and services help engineers address their design, verification, system and manufacturing challenges. Since 1986, engineers around the world have been using Synopsys technology to design and create billions of chips and systems. Learn more at www.synopsys.com.

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