Synopsys Announces Energy-Efficient 28-nm PCI Express 3.0 PHY with Support for 10GBASE-KR

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Highlights:

- Multi-rate PHY IP spans 1.25 Gbps to 10.3 Gbps data rates to cover a broad range of protocols
- Multiprotocol solution supports key standards: PCI Express 3.0, 10GBASE-KR, 10GBASE-KX4, 1000BASE-KX, CEI-6G-SR, SGMII and QSGMII
- Optimized for area and power consumption with support for IEEE's Energy-Efficient Ethernet (EEE) standard to facilitate green enterprise technologies

Synopsys, Inc. (Nasdaq:SNPS), a global leader providing software, IP and services used to accelerate innovation in chips and electronic systems, today announced the availability of its multiprotocol DesignWare® Enterprise 10G PHY IP to address the connectivity needs of a broad range of high-end, energy efficient networking and computing applications. Optimized for long backplane interfaces in server blade chassis, switches, routers and other high-performance computing and networking systems, the 28-nanometer (nm) Enterprise 10G PHY supports multiple interface standards, including PCI Express® (PCIe®) 3.0 and 10GBASE-KR, for a flexible interconnect solution. The new DesignWare IP also implements a multi-lane PHY architecture to support data rates from 1.25 Gbps to 10.3 Gbps per lane, with capabilities to aggregate to 40 Gbps and 100 Gbps Ethernet, giving designers a proven, scalable solution to address the growing demand for additional networking bandwidth in high-speed systems-on-chips (SoCs).

"As the fastest growing protocol in the enterprise and data center market, 10 Gigabit Ethernet is becoming a key backplane interface," said Jag Bolaria, senior analyst at The Linley Group. "Our research indicates over 25% CAGR through 2016 in the number of 10 Gigabit Ethernet ports deployed in the enterprise and data centers. The growth of 10GBASE-KR ports, combined with the rapid adoption of integrated PCI Express 3.0 in multiprocessor cores, elevates the importance of Synopsys' multiprotocol SerDes IP for designers developing ASICs that embed high-speed interfaces."

The DesignWare Enterprise 10G PHY offers a modular design with a highly configurable physical coding sub-layer (PCS) capable of bifurcation and aggregation. Its analog front-end includes multi-tap decision feedback equalization (DFE) and continuous time linear equalization (CTLE), which enhance signal integrity in high throughput communication channels. The DesignWare Enterprise 10G PHY is optimized for area, power and width to ease integration into the rest of the SoC.

The Enterprise 10G PHY is part of Synopsys' complete PCI Express 3.0 and 10G Ethernet solutions, each of which include a PCS, controller and verification IP. The PHY's support for 10GBASE-KR includes physical medium attachment (PMA), auto negotiation (AN), PCS, forward error correction (FEC) and energy-efficient Ethernet (EEE). Providing comprehensive 10GBASE-KR support, including the optional EEE and FEC features, enables SoC designers to single-source IP solutions to help ensure interoperability while reducing risk and time-to-market.

"From the start, we designed the DesignWare Enterprise 10G PHY to enable a flexible range of implementations with scalable data rates, support all major networking and computing protocols, and be available at multiple leading foundries," said John Koeter, vice president of marketing for IP and systems at Synopsys. "Synopsys' complete PCI Express 3.0 and 10G Ethernet IP solutions enable design teams to integrate ultra-high data throughput functionality into their devices with less risk and without compromising time-to-market."

Availability and Resources

- DesignWare Enterprise 10G PHY IP is available now for multiple 28-nm process technologies.
- Learn more about the DesignWare Enterprise 10G PHY
- View the webinar, "Designing to the New PCI Express 3.0 Equalization Requirements"
- Get answers to your 10G Ethernet questions in this video series

About DesignWare IP

Synopsys is a leading provider of high-quality, silicon-proven IP solutions for SoC designs. The broad DesignWare IP portfolio includes complete interface IP solutions consisting of controllers, PHY and verification IP for widely used protocols, analog IP, embedded memories, logic libraries and configurable processor cores. To support software development and hardware/software integration of the IP, Synopsys offers drivers, transaction-level models, and prototypes for many of its IP products. Synopsys' HAPS® FPGA-Based Prototyping

Solution enables validation of the IP and the SoC in the system context. Synopsys' Virtualizer™ virtual prototyping tool set allows developers to start the development of software for the IP or the entire SoC significantly earlier compared to following traditional methods. With a robust IP development methodology, extensive investment in quality, IP prototyping, software development and comprehensive technical support, Synopsys enables designers to accelerate time-to-market and reduce integration risk. For more information on DesignWare IP, visit: http://www.synopsys.com/designware.

About Synopsys

Synopsys, Inc. (Nasdaq:SNPS) accelerates innovation in the global electronics market. As a leader in electronic design automation (EDA) and semiconductor IP, its software, IP and services help engineers address their design, verification, system and manufacturing challenges. Since 1986, engineers around the world have been using Synopsys technology to design and create billions of chips and systems. Learn more at www.synopsys.com.

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