Synopsys' DesignWare STAR Memory System Shipped in 1 Billion Chips

Design Teams Worldwide Quickly Achieve Test and Repair Quality Goals for Embedded Memories

MOUNTAIN VIEW, Calif., Sept. 20, 2011 /PRNewswire/ -- Synopsys, Inc. (Nasdaq: SNPS), a world leader in software and IP used in the design, verification and manufacture of electronic components and systems, today announced that its DesignWare® STAR Memory System® has shipped in one billion chips from semiconductor manufacturers worldwide, reinforcing its status as a trusted test and repair solution for embedded memories. The STAR Memory System is an advanced built-in-self-test (BIST) solution that provides automated pre- and post-silicon memory test, debug and diagnostic capabilities. The automated BIST insertion and advanced repair features reduce design integration time and overall design cost while improving test quality.

"The diagnostic capabilities of Synopsys' STAR Memory System gives us the ability to lower our test costs and improve our manufacturing yield," said Dragos Botea, DFT Manager at SandForce, Inc. "We need a robust, yet economical, integrated test and repair solution to achieve our yield targets and strict quality objectives for our solid state drive processors. The STAR Memory System provides us with the ability to achieve these goals and helps us meet our shrinking product development cycle."

The increasing memory content in system-on-chips (SoCs) is driving the need for high-quality testing to cover all types of memory defects. The STAR Memory System is a complete and cost-effective solution that embeds on-chip memory test and repair logic in SoC designs and can reduce design integration time from months to weeks. Coupled with Synopsys' comprehensive synthesis-based test solution, which also includes TetraMAX® ATPG and DFTMAX™ compression for power-aware scan test, DesignWare SerDes IP with built-in self-test and Yield Explorer for yield analysis, the STAR Memory System, when used in conjunction with DFTMAX compression for logic test, further minimizes the impact on design performance, cost and schedule while meeting overall test cost and quality goals. Enhanced test algorithms provide comprehensive out-of-box fault coverage for advanced process nodes, virtually eliminating test escapes that are typical with generic algorithms.

The STAR Memory System can be used with repairable or non-repairable embedded memories for any foundry or process node to address a broad range of design requirements. Its performance-optimized architecture combined with automated hierarchical embedded test and repair logic insertion and integration capability gives designers ease-of-use and increased productivity in achieving their performance, power, area and test goals. Designers optimize the trade-off between area and advanced diagnostics without sacrificing performance or manufacturing test quality. In addition, advanced transient error fault tolerance enables SoC designers to efficiently address high field-reliability and safety requirements for mission-critical applications.

"With the increasing complexity of integrated circuits and a significant number of memory instances on chips, SoC designers need an integrated memory test and repair system to identify and resolve manufacturing faults," said John Koeter, vice president of marketing for IP and systems at Synopsys. "The broad adoption of Synopsys' silicon-proven STAR Memory System demonstrates the success our customers have had in using the solution to enable high-yielding, memory-rich chips."

Availability

The silicon-proven DesignWare STAR Memory System is available now.

About DesignWare IP

Synopsys is a leading provider of high-quality, silicon-proven IP solutions for SoC designs. The broad DesignWare IP portfolio includes complete interface IP solutions consisting of controllers, PHY and verification IP for widely used protocols, analog IP, embedded memories, logic libraries and configurable processor cores. In addition, Synopsys offers SystemC™ transaction-level models to build virtual prototypes for rapid, pre-silicon development of software. With a robust IP development methodology, reuse tools, extensive investment in quality and comprehensive technical support, Synopsys enables designers to accelerate time-to-market and reduce integration risk. For more information on DesignWare IP, visit: http://www.synopsys.com/designware. Follow us on Twitter at http://twitter.com/designware_ip.

About Synopsys

Synopsys, Inc. (Nasdaq:SNPS) is a world leader in electronic design automation (EDA), supplying the global electronics market with the software, intellectual property (IP) and services used in semiconductor design, verification and manufacturing. Synopsys' comprehensive, integrated portfolio of implementation, verification,

IP, manufacturing and field-programmable gate array (FPGA) solutions helps address the key challenges designers and manufacturers face today, such as power and yield management, system-to-silicon verification and time-to-results. These technology-leading solutions help give Synopsys customers a competitive edge in bringing the best products to market quickly while reducing costs and schedule risk. Synopsys is headquartered in Mountain View, California, and has approximately 70 offices located throughout North America, Europe, Japan, Asia and India. Visit Synopsys online at http://www.synopsys.com

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