Synopsys Extends VMM Methodology for Higher Functional Verification Productivity

Next-Generation VMM Solution Adds Verification Planning, Applications, and Automation to Proven VMM Methodology

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Synopsys, Inc. (NASDAQ: SNPS), a world leader in semiconductor design software, today announced it has extended the industry-leading VMM methodology to enable product development teams to more effectively define, measure and achieve their verification objectives. The next-generation VMM solution delivers higher verification productivity with three new components: VMM Planner, VMM Applications, and VMM Automation. VMM Planner enables managers to systematically plan and track verification progress to increase verification visibility and predictability; VMM Applications reduce testbench creation time by allowing architects to quickly construct more effective verification environments; and VMM Automation improves the productivity of engineers developing and using advanced testbenches. The next- generation VMM solution builds on the proven VMM methodology defined in the popular book Verification Methodology Manual for SystemVerilog.

VMM Planner Increases Verification Visibility and Predictability

Verification planning and tracking are often ad-hoc processes, based on a collection of spreadsheets, documents, reports, log files and emails. This often results in incomplete or inaccurate assessments of the true status of verification and increases the risk of unexpected delays in verification closure.

VMM Planner addresses this challenge by enabling verification teams to systematically capture a feature hierarchy of the design to be verified, together with associated coverage, test, ownership and schedule data, as an executable verification plan. VMM Planner extracts and rolls up a variety of verification results such as code and functional coverage, formal and dynamic assertions, and test pass/fail data, into an annotated plan that can be shared as an accurate, objective and transparent assessment of verification progress.

"The VMM Planner is an important addition to Synopsys' VMM solution, addressing the critical need of chip development teams to have a systematic way of capturing and tracking verification progress," said Randy Mullin, director of verification at Tundra Semiconductor. "The VMM Planner will provide full verification transparency to the chip development team, enabling key milestones to be measured, issues to be quickly identified, and the overall process to become more predictable."

VMM Applications Speed Testbench Creation

VMM Applications provide a collection of high-level functions to further reduce testbench creation time for commonly used design elements, including registers and memories. These new applications are built on the VMM Standard Library, a set of generic building-blocks defined in the Verification Methodology Manual for SystemVerilog. The initial set of VMM Applications includes:

- Register Abstraction Layer to quickly and easily manage verification of thousands of chip configuration registers with automatically-generated tests.
- Hardware Abstraction Layer to create VMM testbenches that can be quickly configured to target simulation or hardware-assisted verification platforms.
- Reusable Environment Composition enables the creation of verification subsystems that can be reused without modification at the system level.
- Memory Allocation Manager to test for potential memory buffer content and address bugs.

"We have seen large verification productivity gains using the Synopsys VMM methodology," said Tim Houlihan, verification manager at Cypress Semiconductor. "We used the VMM Register Abstraction Layer application on our West Bridge Antioch chip and saved two months of effort over a traditional ad- hoc register verification approach. The built-in bit-bash tests were especially helpful in the re-verification required after register set changes."

"The VMM Hardware Abstraction Layer application provides an easy-to-use, high-bandwidth means to connect advanced testbenches to high-performance accelerators and emulators," said Lauro Rizzati, general manager of EVE USA. "By using the Hardware Abstraction Layer's transaction-level interface between the EVE ZeBu emulator and Synopsys' VCS® solution we were able to achieve data transfer rate of more than 500MB per

second data transfer rate."

VMM Automation Improves Verification User Productivity

VMM Automation provides a variety of methodology automation tools and features to improve the productivity of verification users. The VMM SystemC™ transaction level interface provides a high-performance interface between VMM testbenches and SystemC reference models. The VMM Compliance Checker analyzes verification environments against the rules and guidelines from the Verification Methodology Manual for SystemVerilog, providing an easy means to help ensure interoperable and reusable verification components.

"A proven, robust methodology continues to be a key requirement for engineers to realize the power of SystemVerilog for verification" said Manoj Gandhi, senior vice president and general manager of Synopsys' Verification Group. "Synopsys' is extending the proven VMM methodology with the latest addition that enables chip developers to efficiently define, measure and achieve their verification objectives."

Availability

VMM Planner, VMM Applications and VMM Automation will be a part of Synopsys' VCS functional verification solution and Pioneer-NTB testbench automation tool. VMM Planner and VMM Applications are available now in beta; VMM Automation tools will become available over the next 12 to 24 months.

About Synopsys

Synopsys, Inc. is a world leader in EDA software for semiconductor design. The company delivers technology-leading semiconductor design and verification platforms and IC manufacturing software products to the global electronics market, enabling the development and production of complex systems-on-chips (SoCs). Synopsys also provides intellectual property and design services to simplify the design process and accelerate time-to-market for its customers. Synopsys is headquartered in Mountain View, California and has offices in more than 60 locations throughout North America, Europe, Japan and Asia. Visit Synopsys online at http://www.synopsys.com/ .

Forward-Looking Statements

This press release contains forward-looking statements within the meaning of Section 27A of the Securities Act of 1933 and Section 21E of the Securities Exchange Act of 1934, including Synopsys' expectations of the benefits and date of availability of the VMM Solution. These statements are based on current expectations and beliefs. Actual results could differ materially from these statements as a result of unforeseen difficulties in completing the commercial release of the solution, uncertainties attendant to any new product offering and certain statements contained in the section of Synopsys' Annual Report on Form 10-K for the fiscal year ended October 31, 2006 entitled "Risk Factors."

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