Socionext Accelerates Test Generation and Lowers Test Cost Using Synopsys TetraMAX II

TetraMAX II ATPG Speeds Test Generation by 10x and Reduces Patterns by 50 Percent

MOUNTAIN VIEW, Calif., Jan. 16, 2017 /PRNewswire/ --

Highlights:

- TetraMAX II ATPG demonstrated an order-of-magnitude reduction in test generation time from more than a week to days while producing 50% fewer patterns
- Socionext confirmed low-power tests from TetraMAX II ATPG on their upcoming SoC design
- TetraMAX II ATPG ran in Socionext's flow with minimal effort due to compatibility with the previous TetraMAX ATPG solution

Synopsys, Inc. (Nasdaq: SNPS) today announced that Socionext is achieving substantial reduction in test generation time from more than a week to days with TetraMAX® II ATPG, along with 50% fewer patterns, compared to the previous TetraMAX ATPG solution and is planning for usage on a 28-nanometer (nm) SoC design. To meet the company's challenges of achieving high-quality manufacturing test goals with shorter design schedules for their SoC designs, Socionext ran TetraMAX II ATPG with minimal effort to adopt into their flow, and confirmed significantly improved results. TetraMAX II ATPG delivered advanced, hardware-based, low-power test patterns within a few days compared to ten days required by the earlier-generation ATPG. Socionext is collaborating with Synopsys on TetraMAX II ATPG for upcoming SoC designs.

"Our rapid time-to-market and high-quality manufacturing test goals drove us to reassess our ATPG needs," said Taichiro Sasabe, general manager of the SoC design division at Socionext. "As part of our long-term collaboration with Synopsys, we evaluated TetraMAX II and were very pleased that TetraMAX II delivered up to 50% fewer test patterns while running 10x faster than the prior generation TetraMAX ATPG. In addition, we were quickly able to set up TetraMAX II into our design flow because the tool is compatible with TetraMAX. We are confident TetraMAX II will meet our needs for faster, low-power test generation and higher test quality."

TetraMAX II ATPG is built on new engines that are extremely fast, memory efficient, and optimized for generating patterns and diagnosis of defect parts. These innovations led to significantly fewer test patterns and cut runtime from days to hours. TetraMAX II ATPG enables utilization of all server cores regardless of design size, surpassing previous solutions. The ability to reuse production-proven user and tool interfaces ensures designers can quickly deploy TetraMAX II ATPG risk-free on their most challenging designs. TetraMAX II ATPG utilizes established links with Synopsys' Galaxy™ Design Platform tools, such as DFTMAX™ compression, PrimeTime® timing analysis and StarRC™ extraction, as well as other Synopsys tools including Yield Explorer® design-centric yield analysis, to deliver the highest quality test and the fastest, most productive flows.

"Synopsys is addressing the needs of faster time-to-market and higher test quality for all of our customers, such as Socionext," said Bijan Kiani, vice president of product marketing at Synopsys. "Our long-term collaboration with Socionext continues to demonstrate the impactful benefits gained from leveraging state-of-the-art tools and methodologies, such as those delivered by our TetraMAX II ATPG. Following the runtime and quality results Socionext has already seen from their evaluation, we are looking forward to working with them on additional new designs to meet their most challenging test needs."

About the Synopsys Synthesis-Based Test Solution

The Synopsys synthesis-based test solution comprises DFTMAX Ultra, DFTMAX, TetraMAX and TetraMAX II technologies for power-aware logic test and physical diagnostics; DFTMAX LogicBIST for in-system self-test; SpyGlass® DFT ADV for testability analysis; the DesignWare® STAR Hierarchical System for automated hierarchical testing of analog/mixed-signal IP, digital logic blocks, memory and interface IP on an SoC; the DesignWare STAR Memory System® for embedded test, repair and diagnostics; the Z01X™ fault simulator; Yield Explorer design-centric yield analysis; and the Camelot™ software system for CAD navigation. Synopsys' test solution combines Design Compiler® RTL synthesis with embedded test technology to optimize timing, power, area and congestion for test as well as functional logic, leading to faster time-to-results. The Synopsys test solution delivers tight integration across the Synopsys Galaxy Design Platform, including Design Compiler synthesis, IC Compiler™ II place and route, and PrimeTime timing analysis, to enable faster turnaround time while meeting both design and test goals, higher defect coverage and faster yield ramp.

About Synopsys

Synopsys, Inc. (Nasdaq: SNPS) is the Silicon to Software™ partner for innovative companies developing the electronic products and software applications we rely on every day. As the world's 15th largest software company, Synopsys has a long history of being a global leader in electronic design automation (EDA) and semiconductor IP and is also growing its leadership in software security and quality solutions. Whether you're a system-on-chip (SoC) designer creating advanced semiconductors, or a software developer writing applications that require the highest security and quality, Synopsys has the solutions needed to deliver innovative, high-quality, secure products. Learn more at www.synopsys.com.

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