# Synopsys Announces Standards Board Ratification of Its New Parasitic Models for Latest FinFET Process Nodes

Models Available Immediately to Semiconductor and EDA Industries Through a Synopsys Open-source License

MOUNTAIN VIEW, Calif., Sept. 6, 2016 /PRNewswire/ -- Synopsys, Inc. (Nasdaq: SNPS) today announced extensions to its open-source licensed Interconnect Technology Format (ITF), which enables additional modeling of complex parasitic effects between device structures and interconnect layers at the advanced 10-nanometer (nm) and 7-nm process nodes. These new models will enable parasitic extraction tools to accurately capture silicon variation that impacts timing and reliability analysis. Synopsys collaborated with members of the Interconnect Modeling Technical Advisory Board (IMTAB) [member list available at www.imtab.org], an IEEE-ISTO Federation Member Program, to refine and ratify these new extensions. They are available in the Synopsys ITF version 2016 through an open-source license.

"Dealing with increasing variation and complexity at 10-nm and below process nodes requires continuous modeling innovation as well as providing usable standards to facilitate easier adoption," said Bari Biswas, vice president of Engineering for extraction solutions at Synopsys and chair of IMTAB. "Working together with IMTAB members and leading foundries, Synopsys has taken another big step forward by enriching the ITF format with refreshed and extended models to support effects of advanced multi-color patterning and 3D FinFET devices, while ensuring the simplicity to enable efficient enablement and deployment."

The new IMTAB-ratified extensions to ITF include:

- Gate-to-diffusion device parasitic modeling enhancements for required accuracy at 10-nm/7-nm
- Color-aware thickness variation extension for triple and quad color patterning
- Density-aware thickness variation improvement for enhanced modeling of CMP effects
- Silicon coverage-based via resistance for improved accuracy based on silicon dimensions
- Dielectric fill modeling for accurate coupling capacitance extraction of ultra-low dielectrics

"ITF has been embraced by a growing number of leading semiconductor and EDA companies since its inception in 2010 as an interoperable industry standard for parasitic modeling to reduce cost of tool development and speed design cycles," said Marco Migliaro, president, IEEE-ISTO. "The IMTAB consortium's ratification of the latest ITF extensions underscores its commitment to extending these interoperability benefits to advanced 10-nm and 7-nm nodes. IEEE-ISTO looks forward to supporting IMTAB in its mission and commitment to expand the benefits of the ITF common open-source licensed modeling format within the industry."

More information on the new ITF extensions can be found in the ITF specifications version 2016, available at www.synopsys.com/TapIn.

**About ITF**

Synopsys' Interconnect Technology Format (ITF) provides detailed modeling of interconnect parasitic effects that enable designers to perform accurate parasitic extraction for timing, signal integrity, power and reliability signoff analysis. ITF offers a flexible and innovative format to accurately model the effects of increased process variation at advanced process technologies. It is supported by leading semiconductor foundries, integrated device manufacturers and EDA tool providers.

ITF can be licensed for no charge through Synopsys' Technology Access Program (TAP-in™). The latest specifications for ITF can be found at: www.synopsys.com/TapIn.

Requests for ITF enhancements come from the IMTAB membership and the user community.

**About IEEE-ISTO**

IEEE-ISTO is the premier trusted partner of the global technology community for the development, adoption and certification of industry standards. Its mission is to facilitate the life-cycle of industry standards development through a dedicated staff committed to offering vendor neutrality, quality support and member satisfaction. Fostering the market acceptance, adoption and implementation of standardized technologies, IEEE-ISTO programs span the spectrum of today's information and communications technologies. To find out more about IEEE-ISTO, visit www.ieee-isto.org.

**About Synopsys**

Synopsys, Inc. (Nasdaq:SNPS) is the Silicon to Software™ partner for innovative companies developing the electronic products and software applications we rely on every day. As the world's 15th largest software

company, Synopsys has a long history of being a global leader in electronic design automation (EDA) and semiconductor IP, and is also a leader in software quality and security testing with its Coverity® solutions. Whether you're a system-on-chip (SoC) designer creating advanced semiconductors, or a software developer writing applications that require the highest quality and security, Synopsys has the solutions needed to deliver innovative, high-quality, secure products. Learn more at www.synopsys.com.

**Editorial Contacts:**
Sheryl Gulizia
Synopsys, Inc.
650-584-8635
sgulizia@synopsys.com

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