Synopsys Delivers Industry's First Ethernet 400G Verification IP for Next-Generation Networking and Communications Systems

Native SystemVerilog Ethernet VIP Features Built-in Coverage, Verification Planning, Protocol-Aware Debug and Source Code Test Suites

MOUNTAIN VIEW, Calif., Nov. 23, 2015 /PRNewswire/ -- Synopsys, Inc. (NASDAQ: SNPS) today announced the availability of the industry's first verification IP (VIP) and source code test suite to support the proposed IEEE P802.3bs/D1.0 Ethernet 400G standard. As the need for increased bandwidth to support video-on-demand, social networking and cloud services continues to rise, Synopsys VC VIP for Ethernet 400G enables system-on-chip (SoC) teams to design next-generation networking chips for data centers with ease of use and integration, resulting in accelerated verification closure and time to market.

Synopsys VC VIP for Ethernet uses a native SystemVerilog Universal Verification Methodology (UVM) architecture, protocol-aware debug and source code test suites. Synopsys VC VIP is capable of switching speed configurations dynamically at run time and includes an extensive and customizable set of frame generation and error injection capabilities. In addition, source code UNH-IOL test suites are also available for key Ethernet features and clauses, allowing teams to quickly jumpstart their own custom testing and speed up verification time.

"Synopsys is committed to providing a comprehensive Ethernet solution for all speeds, including 25G, 40G, 50G, 100G and the newest 400G standards," said Vikas Gautam, group director of VIP R&D and corporate applications for the Synopsys Verification Group. "Working through our close collaborations with SoC industry leaders, we continue to expand our next-generation Verification IP solutions across all standard protocols."

Availability

Synopsys VC VIP for Ethernet 400G and source code test suites are both available today as early access standalone products.

About Synopsys Verification IP

Synopsys VC VIP, based on its next-generation architecture and implemented in native SystemVerilog and UVM, offers native performance, native debug with Verdi® Protocol Analyzer, ease of use, complete configurability and comprehensive coverage. These capabilities substantially increase user productivity for one of the most difficult and time-consuming aspects of SoC design and verification. The Synopsys VC VIP library includes a broad portfolio of interface, bus and memory protocols. More information is available at www.synopsys.com/vip.

About Synopsys

Synopsys, Inc. (Nasdaq:SNPS) is the Silicon to Software™ partner for innovative companies developing the electronic products and software applications we rely on every day. As the world's 16th largest software company, Synopsys has a long history of being a global leader in electronic design automation (EDA) and semiconductor IP and is also growing its leadership in software quality and security solutions. Whether you're a system-on-chip (SoC) designer creating advanced semiconductors, or a software developer writing applications that require the highest quality and security, Synopsys has the solutions needed to deliver innovative, high-quality, secure products. Learn more at www.synopsys.com.

Editorial Contact:

Sheryl Gulizia
Synopsys, Inc.
650-584-8635
sgulizia@synopsys.com

SOURCE Synopsys, Inc.