Synopsys' New 25G/50G Ethernet Verification IP Enables Next-Generation Gigabit Designs

Native SystemVerilog Ethernet VIP and Source Code Test Suites Enhanced with Built-in-Coverage and Support for Protocol-aware Debug

MOUNTAIN VIEW, Calif., Feb. 3, 2015 /PRNewswire/ -- Synopsys, Inc. (NASDAQ: SNPS), a global leader providing software, IP and services used to accelerate innovation in chips and electronic systems, today announced the availability of verification IP (VIP) for the 25G/50G Ethernet specification developed by the 25 Gigabit Ethernet Consortium. The new VIP is based on native SystemVerilog Universal Verification Methodology (UVM) architecture to enable easy use, easy integration and improved performance. Complete with verification plans, built-in coverage tracking, University of New Hampshire (UNH) compliance test suites, and support for protocol-aware debug with Synopsys' Verdi® Protocol Analyzer, Synopsys VIP for 25G/50G Ethernet provides advanced server and storage endpoint system-on-chip (SoC) teams with a verification IP solution that accelerates verification closure.

"HCL Technologies is one of the fastest growing service companies in the world, bringing IT and engineering services under one roof to solve complex business and product development problems for its clients," said Rajagopal Gunamani, associate vice president of HCL Technologies. "We have collaborated with Synopsys across many projects on the verification of our clients' Ethernet-based SoCs. The release of 25G/50G Ethernet VIP enables us to deliver on verification services as our global customers adopt the latest emerging Ethernet speeds, features and compliance test suites."

"The 25G Ethernet Consortium specification enables high-performance, cost-efficient and scalable interconnects for data center networks with server to top-of-rack links that are able to utilize either a 25G single-lane or 50G dual-lane technology," said Brad Booth, secretary of the 25G Ethernet Consortium. "The release of Synopsys' enhanced Ethernet VIP and its SystemVerilog source code test suites that support the Consortium's 25G/50G Ethernet specification drives faster adoption of this enabling technology."

"The Ethernet standard continues to evolve with significant leaps in speed to meet the functionality of applications in specific market segments, such as server farms. As we continue to collaborate with SoC leaders in this segment, VIP remains an important enabling technology with the advanced features that design teams need to rapidly adopt these new Ethernet specifications," said Debashis Chowdhury, vice president of R&D for the Synopsys Verification Group. "Synopsys has established itself as a technology leader with its SystemVerilog UVM-based verification IP, including UNH test suites for compliance testing. With the release of 25G/50G Ethernet, we provide a leading-edge solution enabling designers to rapidly create and verify differentiated products in the server market."

Availability

Synopsys VIP for 25G/50G Ethernet and UNH test suites is available standalone today, as well as being included in the Synopsys VIP Library and the Verification Compiler™ products. The DesignWare® Enterprise 25G/50G Controller IP is also available now.

About Synopsys Verification IP

Synopsys VIP, based on its next-generation architecture and implemented in native SystemVerilog, offers native performance, native debug with Verdi, enhanced VIP ease of use, configurability, coverage and source code compliance test suites. These capabilities substantially increase user productivity for one of the most difficult and time-consuming aspects of SoC design and verification. Synopsys VIP Library includes a broad portfolio of interface, bus, and memory protocols. More information is available at www.synopsys.com/vip.

About Synopsys

Synopsys, Inc. (NASDAQ:SNPS) accelerates innovation in the global electronics market. As a leader in electronic design automation (EDA) and semiconductor IP, Synopsys delivers software, IP and services to help engineers address their design, verification, system and manufacturing challenges. Since 1986, engineers around the world have been using Synopsys technology to design and create billions of chips and systems. Learn more at www.synopsys.com.

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