Synopsys Bridges Design and Verification with Next-Generation Static and Formal Technology for Verification Compiler

New Formal Verification, Clock Domain Crossing and Low Power Static Checking Products Offer 3X to 5X Performance and Capacity, Ease-of-use and Advanced Debug Needed for Complex SoC Verification

MOUNTAIN VIEW, Calif., June 3, 2014 /PRNewswire/ --

Highlights:

- Next-generation static and formal verification technology now available as part of the Verification Compiler™ product and as standalone solutions
- Solutions provide 3X to 5X better performance and capacity to enable more efficient and effective verification of the largest system-on-chip (SoC) designs
- Seamlessly integrated static and formal verification solutions deliver best-in-class technology, enable ease-of-use, provide unique debug capabilities and are fully compatible with the Synopsys Design Compiler® and Synopsys IC Compiler™ use model and flows
- New static and formal data models, databases and engines provide unparalleled accuracy, greatly reducing violation "noise" and enabling higher productivity and earlier verification closure

Synopsys, Inc. (Nasdaq:SNPS), a global leader providing software, IP and services used to accelerate innovation in chips and electronic systems, today announced the availability of its VC Formal comprehensive formal verification solution, and VC CDC and VC LP advanced static checking solutions. These solutions address the growing verification challenges of complex SoCs by introducing next-generation verification technology that finds bugs earlier, faster and more accurately, as well as accelerates root-cause analysis. VC Formal provides state-of-the-art property checking as well as sequential equivalence checking, connectivity checking and formal coverage analysis. VC CDC provides clock domain crossing verification that is uniquely capable of checking entire SoCs at RTL. VC LP provides low power verification of the most advanced designs based on the Unified Power Format (UPF). The next-generation database and engines offer 3X to 5X performance and capacity compared to previous generation products.

"Aquantia is the market leader in high-speed Ethernet connectivity solutions for cloud computing, data centers and enterprise infrastructure. Low power design is crucial for our award-winning 28 nanometer 10GBASE-T products," said Darren Engelkemier, vice president of digital IC engineering at Aquantia. "Aquantia was one of the first users of Synopsys' next-generation low power static checking technology. VC LP's performance, capacity and ease-of-use simplified our complex low power verification and debug."

"As SoC complexity grows, design and verification teams are increasingly turning to several static and formal verification technologies to expand their verification capabilities. Historically, these teams have been challenged with use-model, debug, performance and capacity limitations," said Prosenjit Chatterjee, GM of North America at Oski Technology. "With VC Formal, VC LP, and VC CDC Synopsys offers a unique approach to combine all these solutions on a single, high-performance, high-capacity data model, with new analysis and debug engines to address many of these traditional challenges."

Synopsys' next-generation static and formal technology is built on a fundamentally new approach—it's architected to broadly support and unify formal techniques, static analysis, simulation and other verification technologies. This unique level of integration and interoperability allows formal verification to work in concert with the other tools and technologies to find bugs faster and more accurately, reduce spurious results and accelerate root- cause determination. In addition, this technology supports new formal/simulation coverage metrics that improve the predictability of verification closure.

Synopsys' next-generation static technology takes full advantage of the incredible capacity and performance offered by new data models and databases to enable checking entire SoCs at RTL flat, allowing these new products to find bugs that previous tools and technologies can't. As an example, deep CDC reconvergence bugs only manifest when the entire SoC is analyzed, which requires enormous capacity. In addition, this technology provides users great flexibility in specifying any type of clock domain crossing synchronizer structure and offers unprecedented power in analyzing these structures for defects or incompleteness. Synopsys' next-generation static and formal technology also leverages common and familiar Design Compiler and IC Compiler use models, greatly shortening the learning curve and flow integration effort associated with previous generation technologies. As a result, users are able to leverage existing Design Compiler and IC Compiler setup scripts to quickly get started with low power and CDC static verification.

"We have been collaborating closely with many customers on our next-generation static and formal verification technologies, which are essential to effectively address the increasing verification challenges of complex SoCs," said Manoj Gandhi, senior vice president and general manager of the Synopsys Verification Group. "We have made a significant investment during the past few years in these leading-edge technologies, which are key elements in Verification Compiler, in order to provide designers with superior static and formal solutions already proven in several successful designs."

Availability

The VC LP solution is scheduled for general availability on June 9, 2014. The VC Formal and VC CDC solutions are scheduled for limited customer availability (LCA) on June 9, 2014. Synopsys' next-generation static and formal verification technology is also included in Synopsys' Verification Compiler product, which is currently in LCA with planned general availability in December 2014.

About Synopsys

Synopsys, Inc. (NASDAQ:SNPS) accelerates innovation in the global electronics market. As a leader in electronic design automation (EDA) and semiconductor IP, its software, IP and services help engineers address their design, verification, system and manufacturing challenges. Since 1986, engineers around the world have been using Synopsys technology to design and create billions of chips and systems. Learn more at www.synopsys.com.

Forward Looking Statements

This press release contains forward-looking statements within the meaning of Section 21E of the Securities Exchange Act of 1934 regarding the expected release and benefits of the Verification Compiler product, VC Formal, VC CDC and VC LP solutions. Any statements that are not statements of historical fact may be deemed to be forward-looking statements. These statements involve known and unknown risks, uncertainties and other factors that could cause actual results, time frames or achievements to differ materially from those expressed or implied in the forward-looking statements. Other risks and uncertainties that may apply are set forth in the "Risk Factors" section of Synopsys' most recently filed Quarterly Report on Form 10-Q. Synopsys undertakes no obligation to update publicly any forward-looking statements, or to update the reasons actual results could differ materially from those anticipated in these forward-looking statements, even if new information becomes available in the future.

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