Synopsys Delivers Industry's Fastest Emulation System

ZeBu Server-3 speeds hardware-software bring-up, OS boot and SoC verification by up to 4X for faster time-to-market on even the largest designs

MOUNTAIN VIEW, Calif., Feb. 25, 2014 /PRNewswire/ --

Highlights:

- High-performance emulation system – run days of system level tests in hours
- Comprehensive debug with full signal visibility and Verdi$^{3™}$ system integration
- Advanced use modes, including power management verification and hybrid emulation with virtual prototypes for architecture optimization and software development
- Advanced architecture for lower total cost of ownership
- Highest capacity – scalable to three billion gates

Synopsys, Inc. (Nasdaq:SNPS), a global leader providing software, IP and services used to accelerate innovation in chips and electronic systems, today announced the availability of ZeBu® Server-3, the industry's fastest emulation system. The Synopsys ZeBu Server-3 builds on the proven ZeBu Server architecture to improve performance by up to 4X and boost capacity by 3X. This performance level enables system-on-chip (SoC) development teams to speed hardware/software bring-up, OS boot and full-chip verification for faster time-to-market.

With its comprehensive debug capabilities, automated software and tight integration with leading verification and system level tool flows, ZeBu Server-3 delivers a highly productive environment for complex SoC verification. It provides multiple verification use modes, including power-aware emulation, simulation acceleration, in-circuit emulation, synthesizable testbench, transaction-based verification (TBV) and hybrid emulation for deployment flexibility based on project requirements. Because of its small footprint, low weight, modest power/cooling requirements and high reliability, ZeBu Server-3 offers lower total cost of ownership of any commercial emulator. ZeBu Server-3 offers the industry's largest design capacity, supporting chips as big as three billion gates with a highly scalable architecture based on high-density 28-nanometer (nm) FPGA technology.

"Advanced multi-core CPU subsystem designs must run huge amounts of software for verification, representing many billions of cycles of testing prior to release," said Charles Matar, Corporate Vice-President, Client SOC Design, at AMD. "We are deploying ZeBu Server-3 for our next-generation CPU subsystem verification because ZeBu's industry-leading emulation performance can help significantly shorten our verification time. In addition, its low total cost of ownership can enable us to easily scale up to larger installations."

"Our networking QorIQ® SoCs with the revolutionary Layerscape™ architecture are designed with a standard, open programming model and a software-aware architecture framework that enables customers to fully exploit the underlying hardware," said Raja Tabet, vice president, Software and Solutions Technology for Freescale Semiconductor's Digital Networking Business. "To create and verify this software framework, our teams need an emulation platform with multi-megahertz performance. That level of design clock performance was achieved with the Synopsys ZeBu Server-3 emulation system. ZeBu's portfolio of modeling transactors coupled with Verdi^3 integration for the debug of our long test scenarios allows us to meet our accelerated software development and validation cycles."

Comprehensive Debug with Full Signal Visibility

ZeBu Server-3 offers simulation-like debug capabilities, including full signal visibility and deterministic rerun, and debug of multi-billion cycle system-level test sequences. Using ZeBu's integration with the popular Synopsys Verdi^3 debug system, users can now quickly analyze waveforms, perform transaction-level debug and access the same powerful debug environment they are familiar with for simulation. ZeBu's interactive Combinatorial Signal Access (iCSA) technology enables users to begin debug with full visibility using Verdi^3 in minutes, rather than in the hours typical of traditional emulation waveform generators. ZeBu's powerful Post Run Debug mode eliminates the constraint of relatively short logic analyzer trace windows, enabling the user to rerun and analyze any scenario deterministically – even scenarios embedded in multi-billion cycle tests – without recompiling the design.

Support for Advanced Verification Use Modes

ZeBu Server-3 supports a wide range of use modes including power management verification, simulation acceleration, embedded testbench, in-circuit emulation (ICE), TBV and hybrid emulation with virtual prototypes

to maximize flexibility across chip development teams with varying requirements. For verification of low-power chips, ZeBu supports IEEE 1801 Unified Power Format (UPF) descriptions for accurate modeling of advanced low-power design constructs and power-aware waveform viewing in Verdi^3. It will also generate switching activity output to enable dynamic power analysis using tools like Synopsys' PrimeTime® PX solution.

Through SystemC TLM 2.0 integration, ZeBu Server-3 supports a hybrid emulation connection to virtual prototypes (like those simulated in Synopsys' Platform Architect™ and Virtualizer™ tools), enabling system architects and software developers to use ZeBu to accelerate architecture optimization and pre-silicon software development. With hybrid emulation, engineers can start software development weeks or months earlier with high-level processor models running in the virtual prototype alongside RTL running in ZeBu, all in one high-performance environment.

Many teams adopt TBV, where the emulator interacts with a virtual test environment on a host computer. Utilizing high-bandwidth, low-latency transactors and a high-speed connection between host and emulator, ZeBu Server-3 can run the SoC at full speed while interacting with the verification environment on the host. ZeBu offers a comprehensive library of transactors, protocol analyzers, virtual devices, virtual speed adapters and pre-compiled memory models that can be used to quickly assemble a transaction-level verification environment. For custom busses or interfaces, the ZeBu ZEMI-3 behavioral SystemVerilog compiler for transactors makes it easy to create cycle-accurate transactors and exchange messages with a high level C++ or SystemVerilog testbench.

Advanced Architecture for Lower Total Cost of Ownership

The performance, capacity, reliability and power-efficiency of an emulator are strongly correlated with the capacity of the chips it uses to represent the design-under-test. Larger emulator chips can generally run the design-under-test at higher speeds, with fewer partitions and lower power-per-gate. Each new generation of ZeBu Server takes advantage of the continued rapid growth in FPGA capacity by adopting the most advanced silicon. The new ZeBu Server-3 continues this approach by utilizing one of the largest devices currently available – the Xilinx Virtex-7 XC7V2000T with 28 nm Stacked Silicon Interconnect (SSI) technology.

Operating an emulator traditionally implies significant expense beyond the initial system purchase. ZeBu Server-3's compact and efficient hardware platform is designed to operate in a standard data center environment with power, cooling and weight requirements consistent with other data center equipment. For example, a 300-million-gate ZeBu Server-3configuration requires just a 20-inch cube of space, consumes only 2.5 kW of peak power and weighs less than 155 pounds – many times lower than required by other emulators with similar capacity. This means that ZeBu Server-3 can usually be installed and used with the existing power and cooling infrastructure in an existing facility rather than requiring expensive construction or space retrofits.

"Verifying an advanced SoC requires a continuum of technologies, with a growing need for higher performance and tighter integration," said Manoj Gandhi, senior vice president and general manager, Verification Group at Synopsys. "We are making a major investment in emulation as part of our overall strategy to help SoC design teams accelerate time-to-market, integrating with future generations of verification technologies including Synopsys' Verdi®, VCS®, and verification IP (VIP) solutions as well as system level tools such as Platform Architect, Virtualizer and our HAPS® solution."

About Synopsys

Synopsys, Inc. (Nasdaq:SNPS) accelerates innovation in the global electronics market. As a leader in electronic design automation (EDA) and semiconductor IP, its software, IP and services help engineers address their design, verification, system and manufacturing challenges. Since 1986, engineers around the world have been using Synopsys technology to design and create billions of chips and systems. Learn more at www.synopsys.com.

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